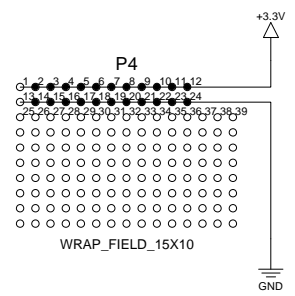
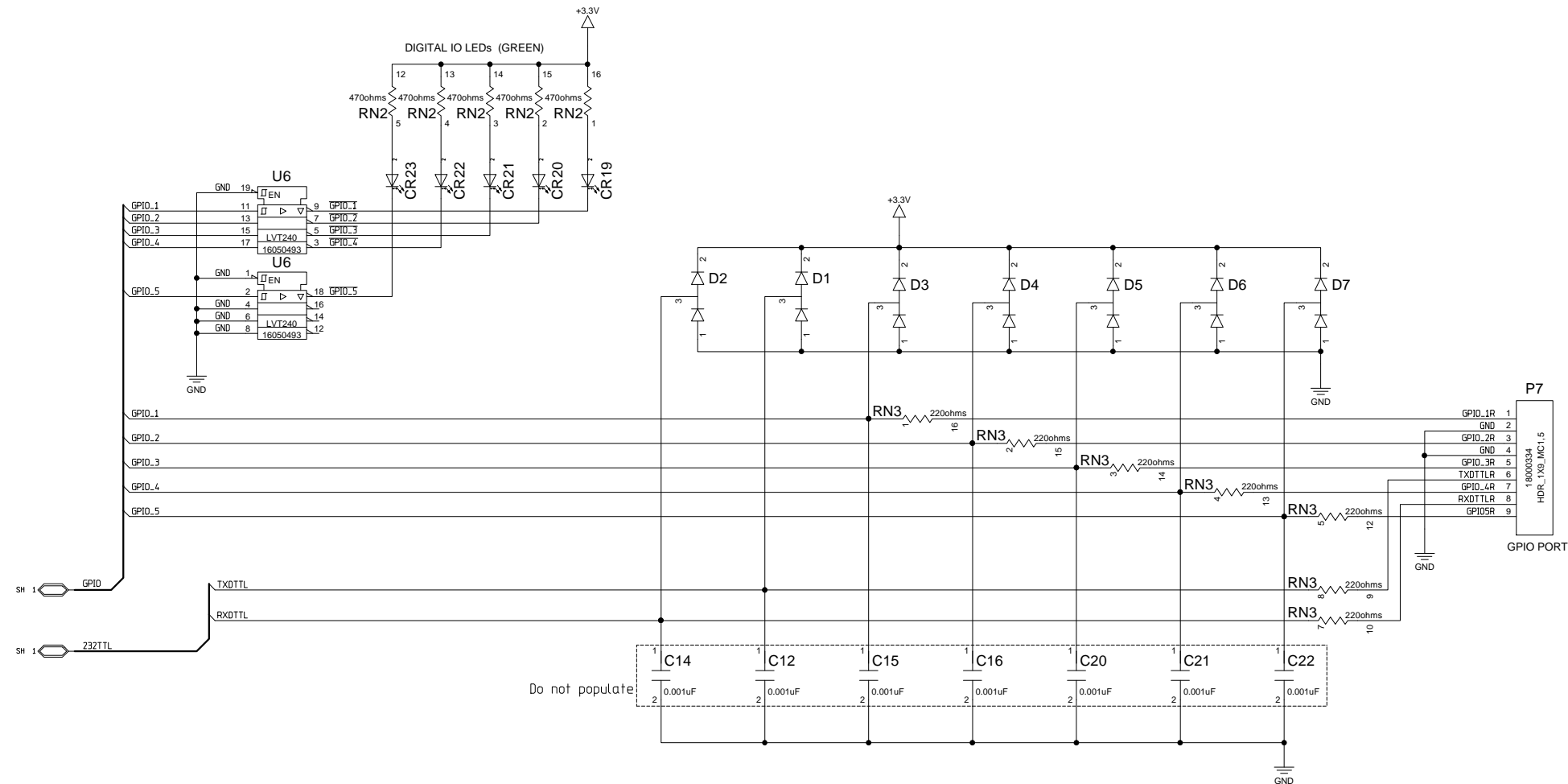


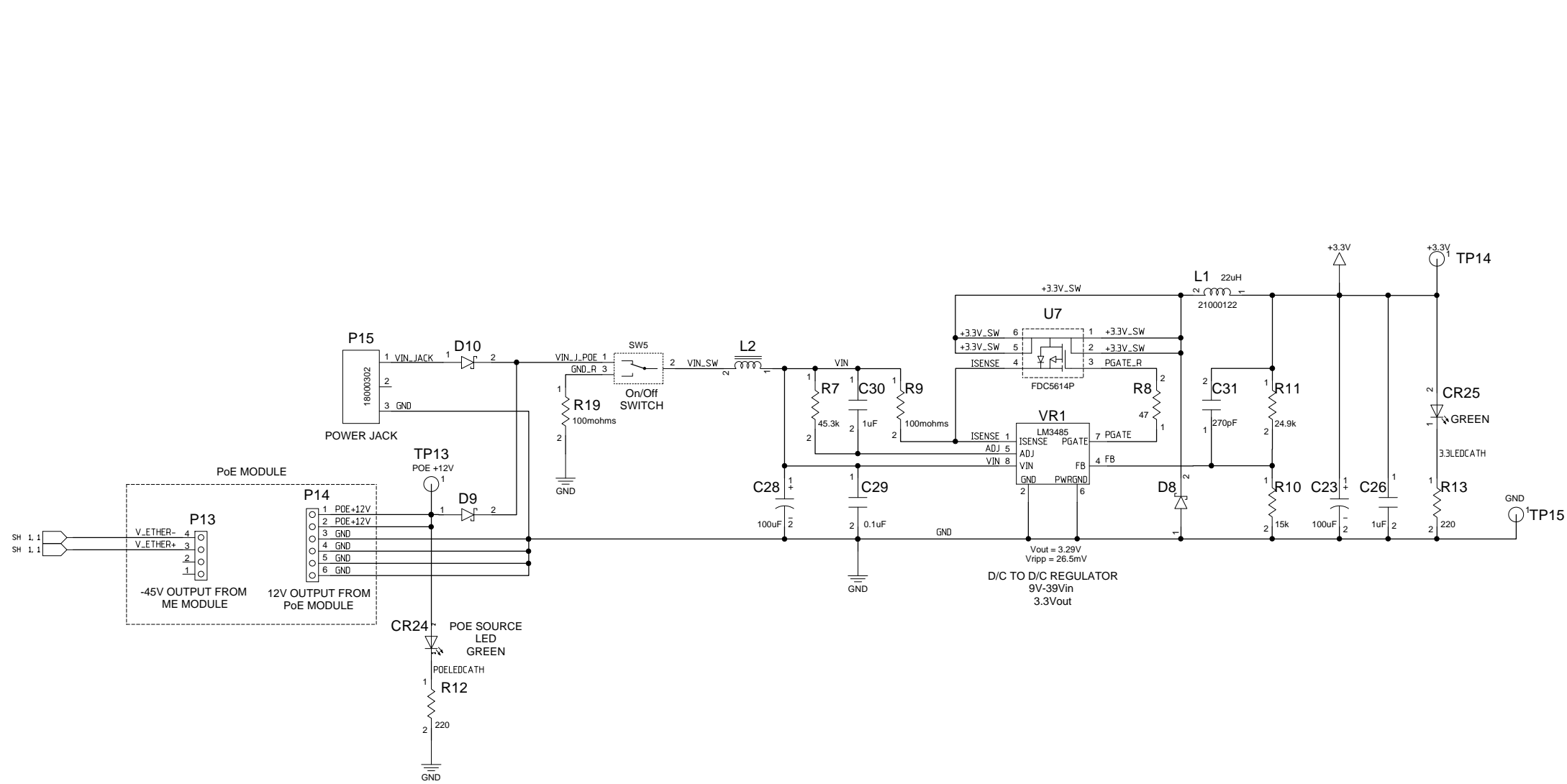
SW3 POSITION

CONTACT #	<input type="checkbox"/>	<input type="checkbox"/>
INPUT 1	DCD	GPIO-1
INPUT 2	CTS	GPIO-2
INPUT 3	DSR	GPIO-3
INPUT 4	RTS	GPIO-4
INPUT 5	DTR	GPIO-5

A	NPR000538	PRODUCTION BUILD			
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR DATE
APPROVALS	DATE				
DESIGNED	8/26/2009				
DRAWN	8/26/2009				
CHECKED	8/26/2009				
ENGINEER	8/26/2009				
11:48:39 AM		SIZE	PART NO.	REV	
		D	30006001-06	A	
DO NOT SCALE DRAWING		SCALE: NTS	VERIBEST	SHEET	01 of 04



REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
A	NPR000538	PRODUCTION BUILD				
APPROVALS		DATE				
DESIGNED	8/26/2009					
DRAWN	8/26/2009					
CHECKED	8/26/2009					
ENGINEER	8/26/2009					
11:48:39 AM		SIZE	PART NO.	REV		
		D	30006001-06	A		
DO NOT SCALE DRAWING			SCALE: NTS	VERIBEST	SHEET 02 of 04	



PCB1
3000001-XX
1
SCHEMATIC
30006001-06 RevA

PCB2
3000002-XX
1
PCB
30006002-06 RevA


ASSEMBLY SHT 1
3000004-XX
1
ASSEMBLY
30006004-06 RevA

A	NPR000538	PRODUCTION BUILD				
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
APPROVALS	DATE					
DESIGNED	8/26/2009					
DRAWN	8/26/2009					
CHECKED	8/26/2009					
ENGINEER	8/26/2009					
11:48:39 AM		SIZE	PART NO.	REV		
DO NOT SCALE DRAWING		D	30006001-06	A		
		SCALE: NTS	VERIBEST	SHEET	03 of 04	

30006001-06 REV A

REASON FOR CHANGES:

1. MAIN REASON IS TO CORRECT THE LAYOUT ISSUE FOR THE SEPARATION BETWEEN P13 AND P14 - POE CONNECTORS.
2. CHANGE SOME OF THE PART NUMBERS OF VARIOUS COMPONENTS TO MATCH THE BOM.
3. ENABLE PRIMARY PORT TRANSCEIVER

A	NPR000538	PRODUCTION BUILD					
REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE	
APPROVALS		DATE	 Digi TITLE: Digi Connect ME Dev Board				
DESIGNED	8/26/2009						
DRAWN	8/26/2009						
CHECKED	8/26/2009						
ENGINEER	8/26/2009						
11:48:39 AM		SIZE	PART NO.	REV			
		D	30006001-06	A			
DO NOT SCALE DRAWING			SCALE: NTS	VERIBEST	SHEET	03 of 04	