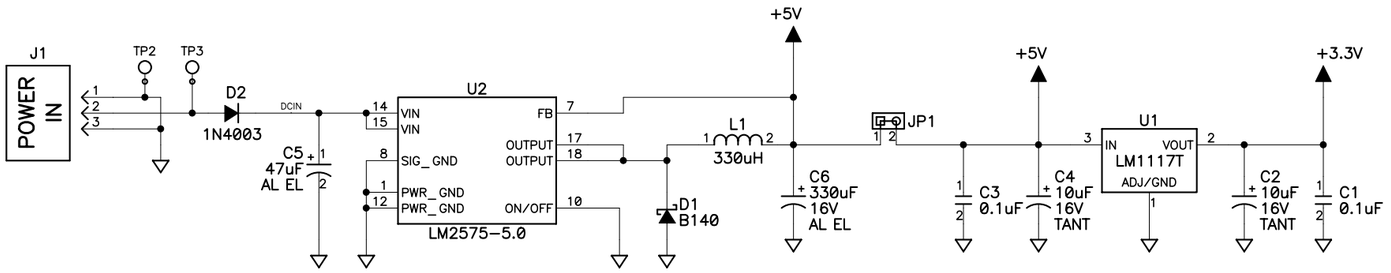
REVISION HISTORY			REVISION APPROVAL			
REV	ECO	DESCRIPTION	PROJECT ENGINEER	APPROVAL DATE	DOCUMENT CONTROL	APPROVAL DATE
A	E14372	INITIAL RELEASE	JC	2/16/06	KF	2/15/06
B	E14875	CHANGE JP11, JP13, JP15, JP17, JP19, JP20, JP21, JP22	JC	10/18/06	KF	10/17/06
C	001119	CHG JP11, JP13, JP15, JP17, JP19–JP22 TO 470 OHMS				



DEFAULT PART INSTALLATION	
PART	
JP11, JP13, JP15, JP17 JP19, JP20, JP21, JP22	470
JP3, JP5, JP7, JP10 JP12, JP14, JP16, JP18	0 Ohm
JP4, JP6, JP8, JP9	NOT INSTALLED
JP1, JP2, JP25	NOT INSTALLED
JP23, JP24	0 Ohm (1–2)
R25	INSTALLED
Q1, R26	NOT INSTALLED

DEFAULT IO ASSIGNMENTS	
Port	Use
PortC[0]	RS–232 T1
PortC[1]	RS–232 R1
PortC[2]	RS–232 T2
PortC[3]	RS–232 R2
PortB[2]	LED, DS2
PortB[3]	LED, DS3
PortB[4]	Switch S2
PortB[5]	Switch S3

NOTES: UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTOR VALUES ARE IN OHMS, 1/16W, 5%
2. ALL CAPACITORS ARE 10VDC OR HIGHER.
3. THE ORIGINATION SOURCE OF A VOLTAGE IS REPRESENTED BY (+V), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY (+V).

4 OUTLINED CIRCUIT MAY NOT BE STUFFED, SEE NOTES.

5. COMPONENT VALUES SHOWN WITH AN ASTERISK (*) FOLLOWING THE VALUE, MAY HAVE DIFFERENT VALUES, OR MAY NOT BE STUFFED DEPENDING ON MODEL.

APPEND THE FOLLOWING DOCUMENTS WHEN CHANGING THIS DOCUMENT:	

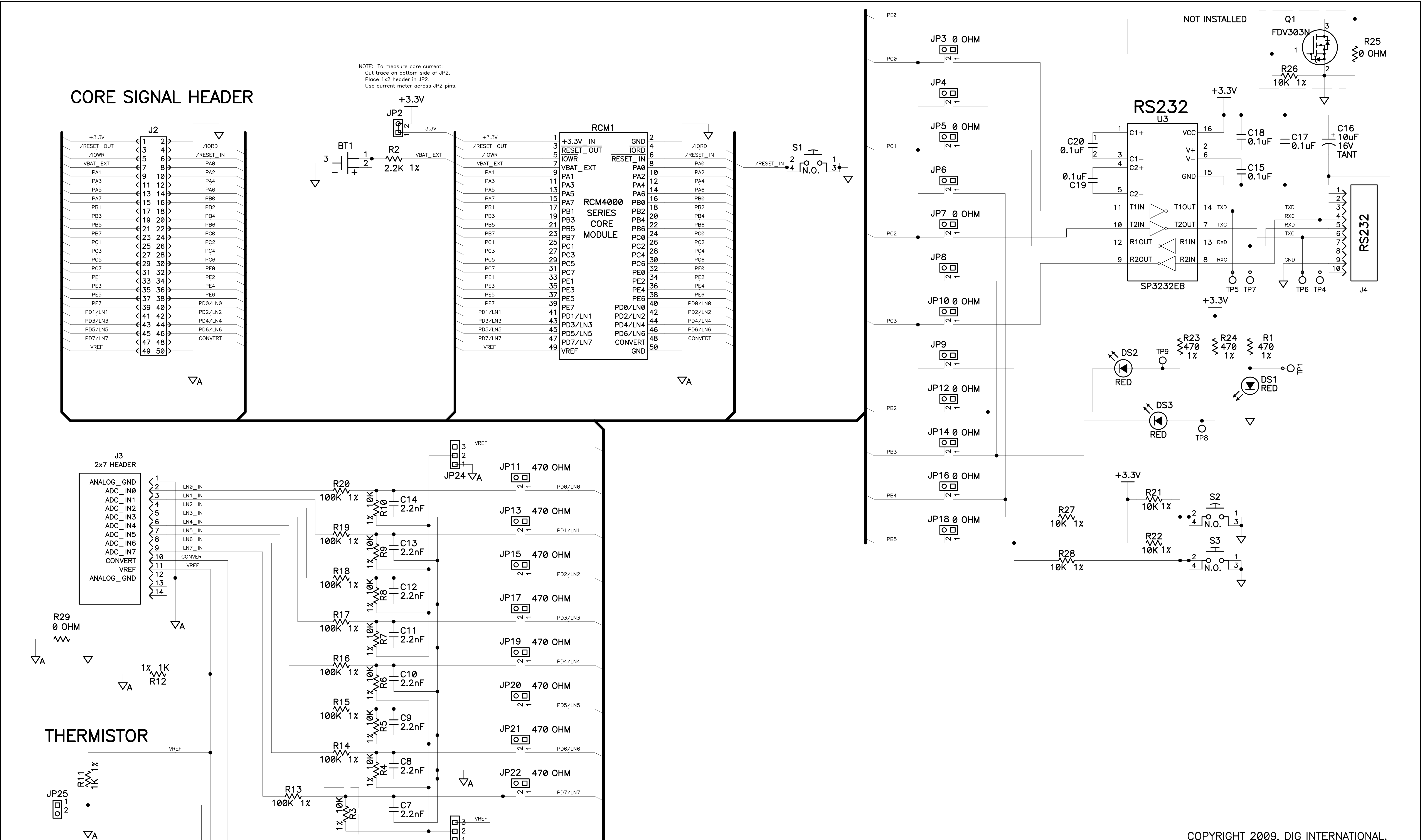
DRAWING CONTENT:	
DRAWN BY: (INITIAL RELEASE) J CAMPBELL	10/16/06
REVISED BY: J NAUER	4/23/09
APPROVALS: INITIAL RELEASE	
PROJECT ENGINEER: J CAMPBELL	1/27/2006
ENGINEERING MANAGER: X TRUONG	
SIGNATURES	DATE

TITLE
SCHEMATIC DIAGRAM
RCM4XXX
PROTO BOARD

RABBIT SEMICONDUCTOR
www.rabbit.com

SIZE **B** DWG NO. 090–0230

SCALE NONE | RELEASE DATE 1/27/06 | SHEET 1 OF 2



SIZE	DWG NO.		
B	090-0230		
SCALE NONE	REV LTR C	SHEET 2	OF 2