30006011-01 REV C

NOTICE!
ECO 580319
NS9750B-A1 WILL NOT accept any clock freq. over 40MHz. See NS9750B-A1 data sheet. Recommended freq. = 29.4912MHz. The PLL is NEVER bypassed.

ECO 580319

Should be 330

See the NS9750 data sheets for the latest crystal/osc circuits

FROM REV A TO B:
POPULATE R541 AND R364 WITH 0 OHM.
ALSO DEPOP R341
SEE ECO 580141

ECO 580319 > See Sheet 2 and the NS9750B-A1 data sheet for the revised JTAG circuit.

DNP = Do Not Populate Items in dashed area not on board.

IMPORTANT Disclaimer!
This power supply design does not meet the latest NS9750 power sequencing requirement. See the NS9750B-A1 data sheet.

ECO 580319

((R2/R1) + 1) * 1.25 = 3.3V

((30.1K/34K) + 1) * 0.8 = 1.508V

ECO 580319
IMPORTANT!

NS9750B-A1:There are 36 new GND pins in a 6x6 array in the middle of the BGA package for a total of 388 balls.
6 pin changes: 1.5V to GND; L23, D18, L4, T23, AC9, T4.
10 pin changes: 3.3V to GND; M23, D19, D8, M4, R23, AC19, AC8, R4

ECO 580319
IMPORTANT!

See the NS9750B-A1 Design Rules for detailed layout recommendations. Available on website-hardwaretoolkit

Alternate 1.5V circuit. (600mA)
Only populate one or the other.

ECO 580319

NOTICE!

TOC and PCB Stack-up added to Sheet 13

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	4 NS9750B-A1 + 3 App. notes				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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TITLE: NS9750 - System and Power

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 01 of 18

BUFFERS - FLASH/STATIC

30006011-01 REV C

SHEET 5 BUFFERED1_A_AND_D
SHEET 4,6 MEM_CONTROL
SHEET 4 ADDRESS
SHEET 3,4 B2_RES
SHEET 3,4 BUFFERED2_A_AND_D
SHEET 4 DATA

ECO 580319

NS9750B-A1

CLKFB[3:0] Inputs have changed

CLKFB0 = CLKIN ((Connect to CLK_OUT(0))

CLKFB1 = SERSET_N (Connect to JTAG SRST_N, pin 15 and to pull-up resistor)

CLKFB2 = ENB_SRESET (Connect to 3.3V)

CLKFB3 = GND (Connect to GND)

ECO 580319
See Sheet 4 for a block diagram of the data bus and the preferred method of connecting the LVC16245 buffers.

U14 MEMORY — NS9750

FOR TEST ONLY — P9 MICTOR38, P8 MICTOR38, P7

U9, U8, U6, U7 — LVC16245A (+3.3V=+3.3V_mem)

RN9, RN10, RN7, RN8, RN3, RN4, RN5, RN6 — 0ohms

U106 7SZU04 — DNP: R547 0ohms

R549 0ohms — DNP: R548 0ohms

C43: C37 C53 C57 C56 C221 C222 C55 C54 C42
C38: C214 C36 C51 C41 C52 C50 C23 C217 C13
C216: C182 C14 C16 C212 C196 C195 C193 C15 C24
C44: C3 C11 C177 C194 C211 C213 C17 C4 C179
C226: C233 C228 C232 C2 C176 C197 C25 C223 C227
0.01uF / 0.1uF — +3.3V_mem — GND

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	1 NS9750B-A1 + 1 App. notes				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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TITLE: NS9750 - Memory

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 02 of 18

30006011-01 REV C

SHEET 2,4 B2_RES

SHEET 2,4 BUFFERED2_A_AND_D

DNP = Do Not Populate

DIMM FOR TEST ONLY
as shown will not allow full
DIMM functionality.
These components not populated

ECO 580319 → **DIMM CKE's**

SDRAM Reset errata:
Always hold SDRAM CKE' S high, OR
use a bus switch to select between
SDRAM CKE with a pull-up resistor and
the NS9750 CKE(x) controlled by reset_done.
reset_done = 1 selects NS9750 CKE to SDRAM.

See the NS9750B-A1 datasheet's JTAG drawing
for an example.

R572 0ohms B2CS(0)~ → CHIP_CS0
R573 0ohms B2CS(0)~ → CHIP_CS1
SW4 SPST8 (B2A(12), B2A(13), B2A(14), B2A(15))
R579 0ohms → BANK_ADDR0
R578 0ohms → BANK_ADDR1

U5 4Mx16 (+3.3V=+3.3V_mem)
B2A(0..11), B2CLKOUT(3), B2CKE(3), CHIP_CS0, B2RAS~, B2CAS~, B2WE~, BANK_ADDR0, BANK_ADDR1
B2D(0..15)
R232 0ohms B2DQM(1)
R228 0ohms DNP
R227 0ohms B2DQM(0)
+3.3V_mem, GND

U4 4Mx16 (+3.3V=+3.3V_mem)
B2A(0..11), B2CLKOUT(3), B2CKE(3), CHIP_CS1, B2RAS~, B2CAS~, B2WE~, BANK_ADDR0, BANK_ADDR1
B2D(16..31)
B2DQM(3), B2DQM(2)
+3.3V_mem, GND

R231 0ohms B2CS(0)~ → DIMM_CS0
R233 0ohms B2CS(1)~ → DIMM_CS1
R30 0ohms B2CS(2)~ → DIMM_CS0
R29 0ohms B2CS(3)~ → DIMM_CS1

R588, R584, R587 10Kohms → +3.3V_mem

P5 DIMM168
+3.3V_mem
B2RD(0..31)
B2RWE~, B2DQM(0), B2DQM(1), DIMM_CS0, B2RA(0..12), BANK_ADDR1, B2CLKDRV(0), B2CKE(2), B2CKE(2)
B2RCAS~, B2RDQM(2), B2RDQM(3), DIMM_CS1, B2RRAS~, B2RA(1), B2RA(3), B2RA(5), B2RA(7), B2RA(9), BANK_ADDR0, B2RA(11), B2CLKDRV(1), B2A(12), DIMM_CLKE, B2A(13)
SDA_DIMM, SCL_DIMM → SHEET 1, SHEET 1
R263 10Kohms → +3.3V_mem
R586 10Kohms, R28 0ohms → GND
R582 10Kohms → GND
R21 0ohms → +3.3V_mem
R22 0ohms → GND

DNP
+3.3V_mem
R581 10Kohms, R585 10Kohms, R583 10Kohms

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	1 App. note				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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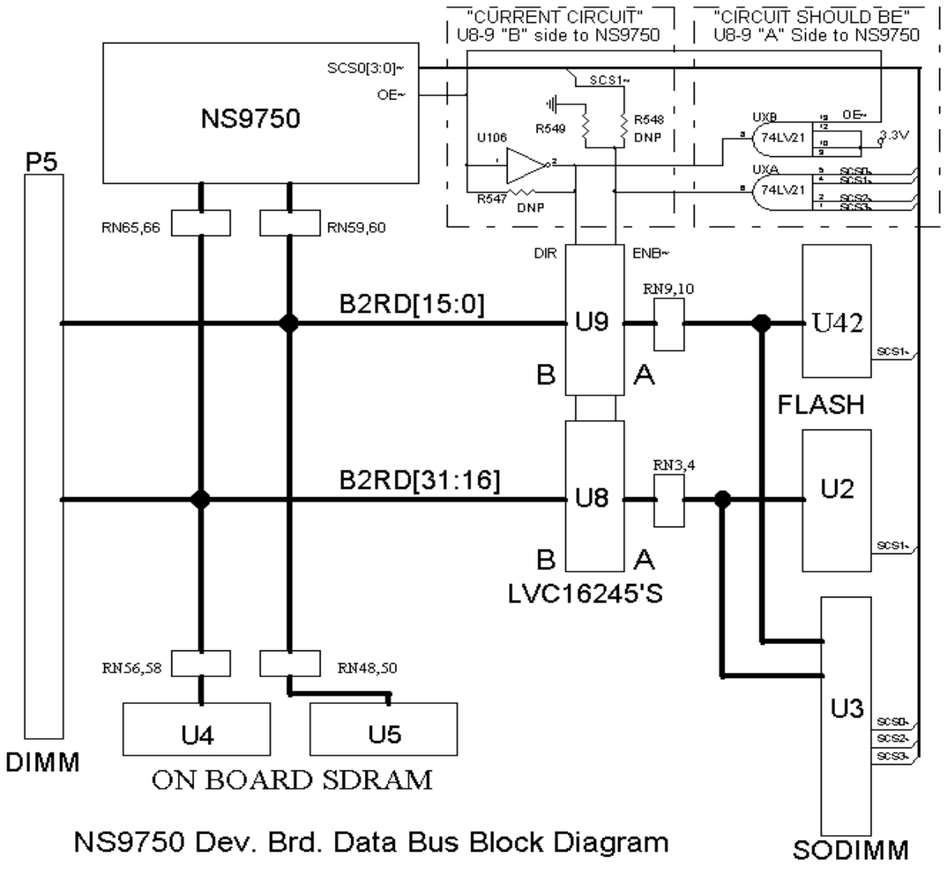
TITLE: NS9750 -SDRAM

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 03 of 18

ECO 580319
Data bus block diagram and preferred method of connecting LVC16245 buffers.



NS9750 Dev. Brd. Data Bus Block Diagram

SHEET 2,3 BUFFERED2_A_AND_D
SHEET 2,3 B2_RES
SHEET 2 DATA
SHEET 2,6 MEM_CONTROL
SHEET 2 ADDRESS

Options for Test

CKE(1) R253 0ohms
CKE(2) DNP R254 0ohms
R264 0ohms B2CKE(2)
CKE(3) R288 0ohms B2CKE(3)
CLKOUT(1) R273 0ohms B2CLKDRV(0)
CLKOUT(2) R280 0ohms B2CLKDRV(1)
CLKOUT(3) R277 47ohms B2CLKOUT(3)

RN59: D(0..7) → B2RD(0..7), 0ohms
RN60: D(8..15) → B2RD(8..15), 0ohms
RN61: DQM(2), WE~, CAS~, DQM(0), CS(0..3)~ → B2RDQM(2), B2RWE~, B2RCAS~, B2DQM(0), B2CS(0..3)~, 47ohms
RN62: RAS~, A(0..6) → B2RRAS~, B2RA(0..6), 47ohms
RN63: A(15), A(14), A(13), A(10), A(9), A(8), A(7), A(12) → B2RA(10), B2RA(9), B2RA(8), B2RA(7), B2RA(12), 47ohms
R574 DQM(1) 47ohms B2DQM(1)
R577 DQM(3) 47ohms B2RDQM(3)
R575 A(11) 47ohms B2RA(11)
RN65: D(16..23) → B2RD(16..23), 0ohms
RN66: D(24..31) → B2RD(24..31), 0ohms

MERC-ID SIDE
Termination will vary by layout, and may not be necessary.

RN48: B2RD(0..7) → B2D(0..7), 0ohms
RN50: B2RD(8..15) → B2D(8..15), 0ohms
RN51: B2RWE~, B2RCAS~, B2RDQM(3), B2RDQM(2), B2RA(7..10) → B2WE~, B2CAS~, B2DQM(3), B2DQM(2), B2A(7..10), 0ohms
RN52: B2RRAS~, B2RA(0..6) → B2RAS~, B2A(0..6), 0ohms
R576 B2RA(11) 0ohms B2A(11)
RN56: B2RD(16..23) → B2D(16..23), 0ohms
RN58: B2RD(24..31) → B2D(24..31), 0ohms

SDRAM SIDE

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	1 App. note				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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TITLE: NS9750 -SDRAM TERMINATION

SIZE D | PART NO. 30006011-01 | REV C

SCALE: NTS | VERIBEST | SHEET 04 of 18

30006011-01 REV C

SHEET 2
SHEET 6,7,9,10,11
BUFFERED1_A_AND_D
GROUP_B

U3
72 - SODIMM
External Peripheral
or SRAM

U42
29W320
+3.3V=+3.3V_mem

U2
29W320
+3.3V=+3.3V_mem

FOR TEST ONLY

U43
AM29LV256M
+3.3V=+3.3V_mem

U1
AM29LV256M
+3.3V=+3.3V_mem

SW1 SPST4
SW3 SPST4
SW2 SPST4

GROUP_D
SHEET 6,8,9,10,11

THIS CIRCUIT AND
HEADER FOR TEST
ONLY
P2,RN1,R5,R8,R9,R10,C9

FLASH DISABLED
WHEN JUMPER
PLACED HERE
JUMPER 1X2 VERTICAL 2MM

ECO 580319
Connect VIO to 3.3V

U27
SOCKET

U28
AT25P1024
SEEPROM

RN93

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	1 App. note				
B	580173	U22 symbol & ECO 580141				

APPROVALS		DATE
DESIGNED	JZ	09/30/2005
DRAWN	JZ	09/30/2005
CHECKED		09/30/2005
ENGINEER	JZ	09/30/2005

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TITLE: NS9750 - FLASH,SRAM,EEPROM

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 05 of 18

30006011-01 REV C

DMA INTERFACE

SPI INTERFACE

ECO 580319
NS9750B-A1does NOT require inverters on serial control lines.

ECO 580319
HDLC INTERFACE IS NOT TESTED OR RECOMMENDED.

TIMERS and INTs USE JUMPER TO LOOP

ECO 580319
GPIO16: USB_OVR is an input in Mode 2 with TIMER11 Mode 0 = RESERVED Output

FOR TEST ONLY

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	1 NS9750B-A1 + 2 App. notes				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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TITLE: NS9750 - GPIO, SPI, HDLC

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 06 of 18

30006011-01 REV C

ECO 580319
NS9750B-A1 does NOT require inverters on serial control lines

ECO 580319
DG412
Pin 04 = V- = -12V
Pin 13 = V+ = +12V
Pin 12 = VL = +5V

PORT A BOTTOM RIGHT

PORT B TOP RIGHT

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	4 App. notes				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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TITLE: NS9750 SERIAL A and B

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 07 of 18

30006011-01 REV C

SW19 SPST4 — RN95 1Kohms — RN94 270ohms 485/232-DR — RN89 270ohms 4W/2W-DR — RN94 270ohms TERM-DR — RN95 1Kohms — RN91 1Kohms — C331 C330 C329 0.1

U101 AND — U36 DG412 (+5V/+5VIO) — TXD_TX485_D(+) — RXD_RX485_D(+) — RI_TXD485_D(-) — DSR_RX485_D(-) — RXD_RX485_D(+)

R531 330 — R532 180ohms — R533 330 — GND — DSR_RX485_D(-)

ECO 580319
DG412
Pin 04 = V- = -12V
Pin 13 = V+ = +12V
Pin 12 = VL = +5V

SW17 SPST4 — RN92 1Kohms — RN90 270ohms 485/232-CR — RN90 270ohms 4W/2W-CR — RN90 270ohms TERM-CR — RN92 1Kohms — RN92 1Kohms — C314 C313 C312 0.1

U90 AND — U37 DG412 (+5V/+5VIO) — TXD_TX485_C(+) — RXD_RX485_C(+) — RI_TXD485_C(-) — DSR_RX485_C(-) — RXD_RX485_C(+)

R528 330 — R529 180ohms — R530 330 — GND — DSR_RX485_C(-)

ECO 580319
DG412
Pin 04 = V- = -12V
Pin 13 = V+ = +12V
Pin 12 = VL = +5V

ECO 580319
NS9750B-A1 does NOT require inverters on serial control lines

U31 NAND — U94 AND — U84 NAND — R461 10Kohms — R460 10Kohms — R501 10Kohms

U117 U130 U135 U119 U116 U136 7SZU04 — 0ohms R611 R624 R629 R613 R610 R630 DNP

DCDDR DSRDR CTSDR~ RIDR DTRDR RTSDR~ RXDDR TXDDR — DCDDRN DSRDRN CTSDRN~ RIDRN DTRDRN RTSDRN~

U80 NAND — 232/485OUTD

C340 C339 C168 C162 C307 C167 C161 C308 0.1

SERIAL_DR — 485/232-DR 4W/2W-DR TERM-DR

RS 422/485 TRANCEIVER U32 MAX3491E — TXD_TX485_D(+) RI_TXD485_D(-) RXD_RX485_D(+) DSR_RX485_D(-) RTS_RTS485_D(+) DTR_RTS485_D(-) CTS_CTS485_D(+) DCD_CTS485_D(-)

232/485OUTD — DCD_CTS485_D(-) RXD_RX485_D(+) TXD_TX485_D(+) DTR_RTS485_D(-) DSR_RX485_D(-) RTS_RTS485_D(+) CTS_CTS485_D(+) RI_TXD485_D(-) — P44 DB9 MALE — PORT D TOP LEFT

+5V +5VIO -12V -12VIO — L16 L45 L44 — TP17 TEST POINT — C346 C175 C345 0.01uF

RS 232 TRANCEIVER U23 MAX3243E — C143 C147 C153 C152 0.1 — R473 47ohms

R459 10Kohms — R458 10Kohms — R500 10Kohms

RS 422/485 TRANCEIVER U91 MAX3491E — U33 MAX3491E — TXD_TX485_C(+) RI_TXD485_C(-) RXD_RX485_C(+) DSR_RX485_C(-) RTS_RTS485_C(+) DTR_RTS485_C(-) CTS_CTS485_C(+) DCD_CTS485_C(-)

232/485OUTC — DCD_CTS485_C(-) RXD_RX485_C(+) TXD_TX485_C(+) DTR_RTS485_C(-) DSR_RX485_C(-) RTS_RTS485_C(+) CTS_CTS485_C(+) RI_TXD485_C(-) — P44 DB9 MALE — PORT C BOTTOM LEFT

C315 C316 C163 C166 C164 C165 0.1

U29 NAND — U83 AND — U100 NAND

U131 U134 U128 U132 U133 U129 7SZU04 — 0ohms R625 R628 R622 R626 R627 R623 DNP

DCDCR DSRCR CTSCR~ RICR DTRCR RTSCR~ RXDCR TXDCR — DCDCRN DSRCRN CTSCRN~ RICRN DTRCRN RTSCRN~

GROUP_C — SHEET 6,9,10,11

GPIO(23) R463 DCDCR — GPIO(41) R153 RXDCR — GPIO(21) R462 DSRCR — GPIO(43) R451 CTSCR~ — GPIO(22) R152 RICR — GPIO(40) R484 TXDCR — GPIO(20) R176 DTRCR — GPIO(42) R194 RTSCR~ — GPIO(36) R163 485/232-CR — GPIO(37) R178 4W/2W-CR — GPIO(38) R165 TERM-CR — DNP

SHEET 5,6,9,10,11 — GROUP_D

SERIAL_DR — DNP R164 R474 R155 R464 R154 R518 — R519 R177 R195 R502 R483 — TERM-DR 4W/2W-DR 485/232-DR RTSCR~ DTRDR — GPIO(27) GPIO(45) GPIO(25) GPIO(47) GPIO(26) GPIO(44) — GPIO(16) GPIO(49) GPIO(48) GPIO(46) GPIO(24)

RS 232 TRANCEIVER U24 MAX3243E — C144 C148 C155 C154 0.1 — R472 47ohms

NAND U79

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	4 App. notes				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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TITLE: NS9750 SERIAL C and D

SIZE D | PART NO. 30006011-01 | REV C

SCALE: NTS | VERIBEST | SHEET 08 of 18

CONFIGURATION SWITCHES

SHEET 01 CONFIG
SHEET 5,6,8,10,11 GROUP_D
SHEET 6,8,10,11 GROUP_C
SHEET 6,7,10,11 GROUP_A
SHEET 5,6,7,10,11 GROUP_B

If USB PNP does not work and PCI is not used or processor full speed is not required, a user could turn SW11-5 to on.

SW10 / RN88: RTCK_OUT, BOOT_STRAP(4), BOOT_STRAP(3), BOOT_STRAP(2), BOOT_STRAP(1), BOOT_STRAP(0), GPIO(49), GPIO(44) — SPST8 — PCI_INT_EXT, 32b_8b_OR_16b, 8b(32)_16b, CLK_DLY_CMD_DLY, PCI_CARDBUS, WE_BW_BL_EN, CS_LO_CS_HI, LITTLE_BIG_ENDIAN — 2.7Kohms

SW11 / RN87: RST_DONE, GPIO(24), GPIO(20), GPIO(19), GPIO(17), GPIO(12), GPIO(10), GPIO(8) — SPST8 — FLASH_EE_BOOT, IS(1), IS(0), PLL_BYPASS, ND(4), ND(3), ND(2), ND(1) — 2.7Kohms

SW12 / RN86: GPIO(4), GPIO(2), GPIO(0), GPIO(41), GPIO(40), GPIO(39), GPIO(38), GPIO(37) — SPST8 — ND(0), FS(1), FS(0), GP31, GP30, GP29, GP28, GP27 — 2.7Kohms

SW13 / RN85: GPIO(36), GPIO(35), GPIO(34), GPIO(33), GPIO(32), GPIO(31), GPIO(30), GPIO(29) — SPST8 — GP26, GP25, GP24, GP23, GP22, GP21, GP20, GP19 — 2.7Kohms

SW14 / RN84: GPIO(28), GPIO(27), GPIO(26), GPIO(25), GPIO(23), GPIO(22), GPIO(21), GPIO(18) — SPST8 — GP18, GP17, GP16, GP15, GP14, GP13, GP12, GP11 — 2.7Kohms

SW15 / RN83: GPIO(16), GPIO(15), GPIO(14), GPIO(13), GPIO(11), GPIO(9), GPIO(7), GPIO(6) — SPST8 — GP10, GP09, GP08, GP07, GP06, GP05, GP04, GP03 — 2.7Kohms

SW16 / RN82: GPIO(5), GPIO(3), GPIO(1), PLLTEST-, BISTEN-, SCANEN-, PLLTEST-, BISTEN- — SPST8 — GP02, GP01, GP00, PLLTEST_LO, BISTEN_LO, SCAN_EN_LO, PLLTEST_HI, BISTEN_HI — 2.7Kohms

SW ITCH OFF / SW ITCH ON

internal PCI arbiter / external PCI arbiter
32 bits wide CS1 / 8 or 16 bits CS1
8 bits (32 bits) CS1 / 16 bits CS1
clock delayed mode / command delayed mode
PCI mode / Cardbus mode
write_en for byte wide devices / byte lane enable
active low chip select / active high chip select
little endian / big endian

boot from flash / boot from SDRAM w/SPI EEPROM
both off = ND is 16:31, sw2 off = ND is 8:15
sw3 off = ND is 4:7, both on = ND 0:3
PLL not bypassed / PLL bypassed

ND(4-0) control PLL multiplier. DEFAULT is 27. please see NS9750 Data Sheet - Table 1.

NOTICE!
ECO 580319
NS9750B-A1
PLL MUST NOT be Bypassed

SHEET 6 USB

FS(1) and FS(0) select Frequency. See Data Sheet for Details

GP31 through GP0 are a general purpose, user defined ID register

DEFAULT= ARM DEBUG
SW4=OFF,SW5=OFF, SW6=ON
SW7=ON,SW8=ON

FOR NORMAL OPERATION
SW4=OFF,SW5=ON, SW6=ON
SW7=ON,SW8=OFF

R453 10K, R452 10K, R161 10K (1 DNP)

GPIO(16), GPIO(17) — R144 0ohms DNP, R143 0ohms — U72, U73, U74, U75, U76 (AND) — CR6, CR5, CR4, CR3, CR2 — R443, R444, R445, R446, R447 330ohms

R448 330ohms, CR1 Power LED, +3.3V, GND

L59 GND, C386 0.01uF, +3.3VuP, +3.3V_INV

R137 0ohms GPIO(17) USB_PWR

R136 0ohms GPIO(16) USB_OVR — U21 7SZU04

R411 10Kohms, R410 0ohms, C302 0.1uF — OPTIONAL RC FILTER FOR OVER CURRENT CAN REMOVE PU IF FILTER NOT USED

R298 100ohms, U68 +3.3V=+3.3Vusb, R315 10Kohms, +3.3VuP

U110 LVC2G04 +3.3V=+3.3V_INV, R297 0ohms, DNP U110 LVC2G04, R289 1.5Mohms, X2 48MHz, C268 10pF, C254 10pF, R282 0ohms, USB_X1, USB_X2

R282 should be 100

ECO 580319
L30 should connect to USB_X1 side (R297)
See the NS9750B-A1data sheet for latest USB clock circuits.

L30 1.0uH, 100pF, 62ohms, C258, R299

USB_D-, USB_D+ — R148 25.5ohms, R149 25.5ohms

D10, D9, D2

C140 22pF, C141 22pF

SWITCH 2 ON FOR USB DEVICE
SWITCH 4 ON FOR SLOW SPEED DEVICE
SWITCH 1 AND 3 ON FOR USB HOST
ONLY ONE SETTING MAY BE USED.

SW9 SPST4

C334, C317, C142, C321, C305, C160, C333 0.1uF / 0.01uF

+5V, L13, C130 0.1uF

ECO 580319
This design allows USB power to be ON following power-up until code sets up USB registers, and sets GPIO[17] to mode 0. GPIO[17] cannot be pulled down since it is a bootstrap that effects bus speed.
Additional logic and another GPIO can be added to prevent this. See example.

GPIO[xy], 2.4K, GPIO[17], NAND2, USB_PWR — To ENABLE~ of a TPS2041 instead of a TPS2051

U22 TPS2051 — IN1, IN2, EN, OC, OUT1, OUT2, OUT3, GND
EARLIER VERSION HAD PIN 4 EN SHOWN ACTIVE LOW. CORRECT TO ACTIVE HIGH REV B

C303 0.1uF, C129 220uF

D3, D11, C325 1uF, R166 470Kohms

VR4 TPS76933 — Vin, Vout, EN, NC/FB, GND — +3.3V_USB, C324 10uF YSU 1206

R139 0ohms DNP, GPIO(17), USB_EN

TP16 TEST POINT, TP15 TEST POINT, L14, L12

R167 4.99ohms, R147 1.5Kohms DNP, C151 0.01uF

USB HOST P31 — PWR, DM0, DP0, USB_GND, SHIELD — USB TYPE A

L39, USB_SHIELDA, USB_SHIELDB

P32 USB DEVICE — PWRB, DM0, DP0, USB_GND, SHIELD — USB TYPE B

L41, L42, C318 0.01uF

R466 1.5Kohms, R467 1.5Kohms, R468 15Kohms, R469 15Kohms, +3.3V_USB

C306 0.01uF

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	2 NS9750B-A1 + 1 App. notes				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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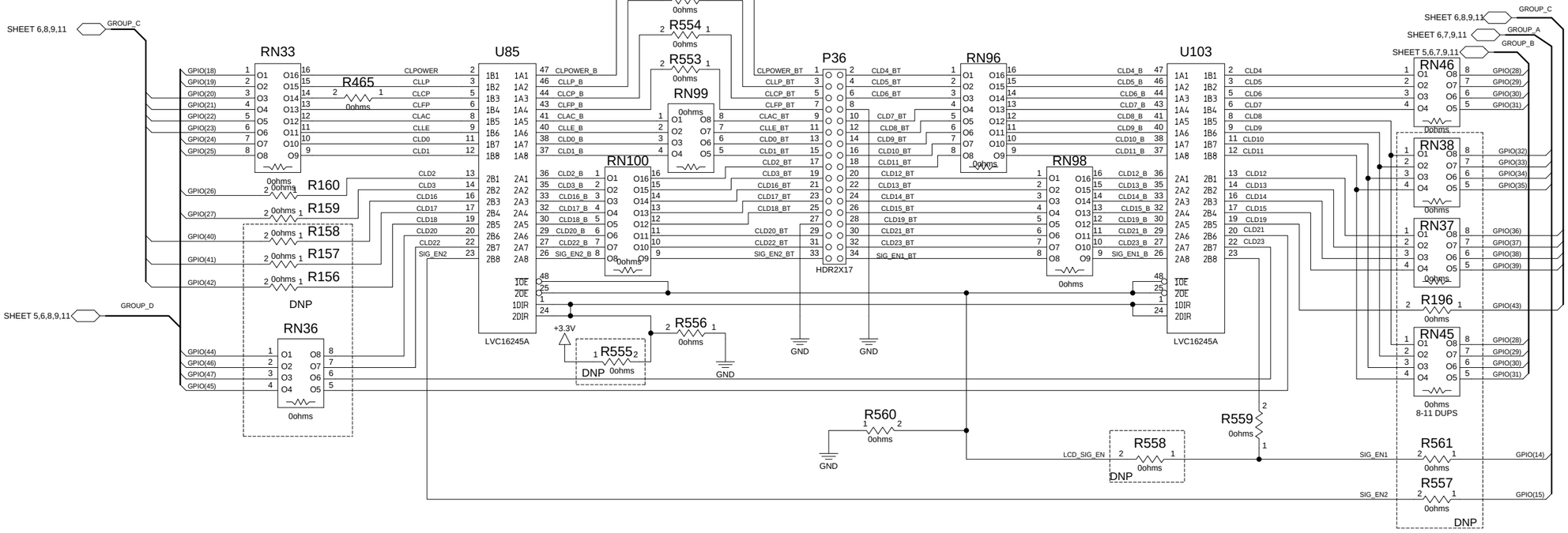
TITLE: NS9750, CONFIG, USB

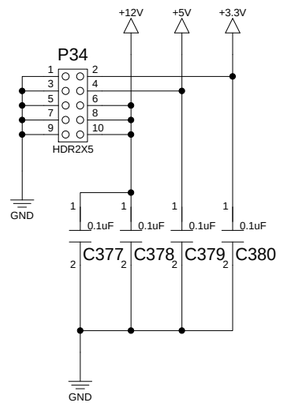
SIZE	PART NO.	REV
D	30006011-01	C

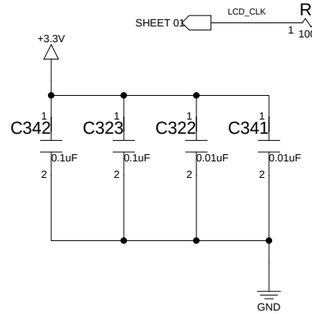
SCALE: NTS | VERIBEST | SHEET 09 of 18

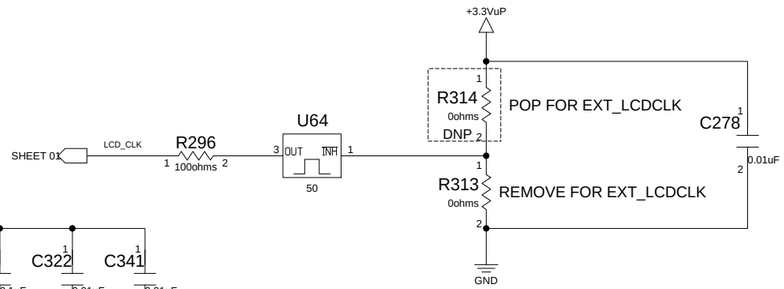
30006011-01 REV C

30006011-01 REV C









REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	No changes				
B	580173	U22 symbol & ECO 580141				

APPROVALS	DATE	Digi
DESIGNED WJR	09/30/2005	
DRAWN WJR	09/30/2005	TITLE: NS9750 - LCD
CHECKED	09/30/2005	
ENGINEER WJR	09/30/2005	SIZE D / PART NO. 30006011-01 / REV C
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30006011-01 REV C

U14
RESERVED
1.5VCORE
3.3VIO
TIE TO GROUND
RES1 RES2 RES3 RES4 RES5 RES6 RES7 RES8 RES9 RES10 RES11 RES12 RES13 RES14 RES15
NO CONNECTS
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8
NS9750

+1.5V +3.3VuP
R312 0ohms
R330 0ohms
AD4 AF2
J1 K3 K2 K1 R1 R2 R3 T1 AF6 AE3 AC5 M2 M1 N2
L3 L2 L1 M3 AE7 AF22 AD21 AE22
RN71 RN69 0ohms
GND

FOR TEST ONLY
DNP P10
MICTOR38
SCL SDA
SHEET 1 SHEET 1

SHEET 6,8,9,10 GROUP_C
SHEET 6,7,9,10 GROUP_A
SHEET 5,6,8,9,10 GROUP_D
SHEET 5,6,7,9,10 GROUP_B
RN34 RN35 0ohms
GPIO(32) GPIO(33) GPIO(34) GPIO(35) GPIO(36) GPIO(37) GPIO(38) GPIO(39)
GPIO(3) GPIO(4) GPIO(5) GPIO(44) GPIO(6) GPIO(45) GPIO(46) GPIO(47)
R538 R544 R478 R540 R535 R539 0ohms
GPIO(48) GPIO(16) GPIO(49) GPIO(28) GPIO(29) GPIO(30)
DNP
U104 7SZU04
1284D0 1284D1 1284D2 1284D3 1284D4 1284D5 1284D6 1284D7
1284nACK 1284BUSY 1284PERROR 1284SELECT 1284PFLT 1284nSTROBE 1284nAUTOFD 1284nINIT 1284nSELECTIN
1284PLOGIC
+3.3V
HIGH DRIVE R537 2.7Kohms
LOW DRIVE R536 0ohms DNP
GND

D12
C352 0.1uF
DNP L48
L49
C388 C389 0.1uF
+5V +3.3V
U40
VCC1 VCC_C1 VCC2 VCC_C2
LVX161284A
U41
VCC
PACSZ1284
GND

P42
1284STROBE_B 1284D1_B 1284D2_B 1284D3_B 1284D4_B 1284D5_B 1284D6_B 1284D7_B 1284D8_B 1284ACK_B 1284BUSY_B 1284PERROR_B 1284SELECT_B 1284AUTOFD_B
1284_SHIELD 1284CENT_PWR_B
C353 0.01uF DNP
L51
1284_SHIELD
CENTRONICS
1284INIT_B 1284FAULT_B 1284SELECTIN_B
1284_SHIELD 1284_SHIELD
GND

+5V +1.5V +3.3V
C220 C247 C245 C234 C172 C292 C343 C344
0.1uF 0.01uF
GND

PARALLEL 1284 INTERFACE

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	No changes				
A	580124	Release				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
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TITLE: NS9750 -1284, RESERVED

SIZE	PART NO.	REV
D	30006011-01	C

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30006011-01 REV C

+3.3V_PCI1

RN73 — RN77 — 10Kohms

R293 10Kohms, R325 10Kohms, DNP R272 10Kohms

Res values to be between 4.8K and 45Kohm, as specified per 5.3.3.3.1 if Cardbus spec. Rmax determined by # of loads present.

INTC# populated if using standard PCI connectors on back of board.

PCI_GNT2~ PCI_REQ2~ PCI_GNT3~ PCI_REQ3~ PCI_RESET~ PCI_INTA~ PCI_INTB~ PCI_GNT1~ PCI_REQ1~ PCI_FRAME~ PCI_IRDY~ PCI_TRDY~ PCI_STOP~ PCI_SERR~ PCI_DEVSEL~ PCI_PERR~ PCI_INTD~ PCI_INTC~

PCI_CTRL

PCI_AD

U14 PCI — NS9750

PCI_CBE(0)	L25	CBE0	AD0	J24	PCI_AD(0)
PCI_CBE(1)	P25	CBE1	AD1	H26	PCI_AD(1)
PCI_CBE(2)	U25	CBE2	AD2	J25	PCI_AD(2)
PCI_CBE(3)	AA26	CBE3	AD3	J26	PCI_AD(3)
			AD4	K24	PCI_AD(4)
PCI_DEVSEL~	T26	DEVSEL	AD5	K25	PCI_AD(5)
PCI_FRAME~	U26	FRAME	AD6	K26	PCI_AD(6)
PCI_IDSEL	Y25	IDSEL	AD7	L24	PCI_AD(7)
PCI_TRDY~	T25	TRDY	AD8	L26	PCI_AD(8)
PCI_IRDY~	T24	IRDY	AD9	M24	PCI_AD(9)
			AD10	M25	PCI_AD(10)
PCI_GNT1~	AC24	GNT1	AD11	M26	PCI_AD(11)
PCI_GNT2~	AD23	GNT2	AD12	N24	PCI_AD(12)
PCI_GNT3~	AE24	GNT3	AD13	N25	PCI_AD(13)
PCI_REQ1~ NOTE 3	AD25	REQ1	AD14	N26	PCI_AD(14)
PCI_REQ2~ NOTE 4	AB23	REQ2	AD15	P26	PCI_AD(15)
PCI_REQ3~ NOTE 3	AC22	REQ3	AD16	U24	PCI_AD(16)
PCI_INTA~ NOTE 3,4	AF25	INTA	AD17	V26	PCI_AD(17)
PCI_INTB~ NOTE 3	AF24	INTB	AD18	V25	PCI_AD(18)
PCI_INTC~ NOTE 3,4	AE23	INTC	AD19	W26	PCI_AD(19)
PCI_INTD~ NOTE 3	AD22	INTD	AD20	V24	PCI_AD(20)
			AD21	W25	PCI_AD(21)
PCI_RESET~	AE26	RESET	AD22	Y26	PCI_AD(22)
			AD23	W24	PCI_AD(23)
PCI_CLKIN	AB24	CLKIN	AD24	Y24	PCI_AD(24)
PCI_CLK	AA23	CLK	AD25	AA25	PCI_AD(25)
			AD26	AB26	PCI_AD(26)
PCI_PERR~ NOTE 11,12	R25	PERR	AD27	AA24	PCI_AD(27)
PCI_PAR	P24	PAR	AD28	AB25	PCI_AD(28)
PCI_SERR~	R26	SERR	AD29	AC26	PCI_AD(29)
PCI_STOP~	R24	STOP	AD30	AD26	PCI_AD(30)
HOST_SEL	AF23	RSC_IN	AD31	AC25	PCI_AD(31)

MICTOR38 — P11 DNP — GND

PCI_GNT2~ PCI_REQ2~ PCI_GNT3~ PCI_REQ3~ PCI_INTB~ PCI_INTA~ PCI_RESET~ PCI_INTC~ PCI_REQ1~ PCI_AD(20) PCI_AD(17) PCI_PAR PCI_AD(18) PCI_INTD~ PCI_AD(31) PCI_AD(29) PCI_GNT1~ PCI_AD(27) PCI_AD(25) PCI_AD(30) PCI_AD(28) PCI_CBE(3) PCI_AD(23) PCI_AD(26) PCI_AD(21) PCI_AD(24) PCI_AD(19) PCI_AD(22) PCI_IDSEL

MICTOR38 — P16 DNP — FOR TEST ONLY — GND

PCI_CBE(2) PCI_AD(16) PCI_IRDY~ PCI_FRAME~ PCI_TRDY~ PCI_STOP~ PCI_SERR~ PCI_DEVSEL~ PCI_PERR~ PCI_AD(15) PCI_CBE(1) PCI_CLK PCI_INTD~ ARBITER_SEL HOST_SEL CARDTYPE_SEL

PCI_AD(13) PCI_AD(11) PCI_AD(9) PCI_CBE(0) PCI_AD(14) PCI_AD(12) PCI_AD(10) PCI_AD(8) PCI_AD(13) PCI_AD(11) PCI_AD(9) PCI_CBE(0) PCI_AD(14) PCI_AD(12) PCI_AD(10) PCI_AD(8)

PCI_TRDY~ PCI_STOP~ PCI_SERR~ PCI_DEVSEL~ PCI_PERR~ PCI_AD(15) PCI_CBE(1) PCI_TRDY~ PCI_STOP~ PCI_SERR~ PCI_DEVSEL~ PCI_PERR~ PCI_AD(15) PCI_CBE(1)

PCI_AD(20) PCI_AD(17) PCI_PAR PCI_AD(18) PCI_CBE(2) PCI_AD(16) PCI_IRDY~ PCI_FRAME~ PCI_AD(20) PCI_AD(17) PCI_PAR PCI_AD(18) PCI_CBE(2) PCI_AD(16) PCI_IRDY~ PCI_FRAME~

PCI_CBE(3) PCI_AD(23) PCI_AD(26) PCI_AD(21) PCI_AD(24) PCI_AD(19) PCI_AD(22) PCI_IDSEL PCI_CBE(3) PCI_AD(23) PCI_AD(26) PCI_AD(21) PCI_AD(24) PCI_AD(19) PCI_AD(22) PCI_IDSEL

PCI_REQ1~ PCI_AD(31) PCI_AD(29) PCI_GNT1~ PCI_AD(27) PCI_AD(25) PCI_AD(30) PCI_AD(28) PCI_REQ1~ PCI_AD(31) PCI_AD(29) PCI_GNT1~ PCI_AD(27) PCI_AD(25) PCI_AD(30) PCI_AD(28)

PCI_GNT2~ PCI_REQ2~ PCI_GNT3~ PCI_REQ3~ PCI_INTB~ PCI_INTA~ PCI_RESET~ PCI_INTC~ PCI_GNT2~ PCI_REQ2~ PCI_GNT3~ PCI_REQ3~ PCI_INTB~ PCI_INTA~ PCI_RESET~ PCI_INTC~

PCI_INTD~ ARBITER_SEL HOST_SEL CARDTYPE_SEL PCI_INTD~ ARBITER_SEL HOST_SEL CARDTYPE_SEL

+3.3VuP — R307 0ohms — U67 NOTE 6 — INH OUT — 33 +3.3V=+3.3VuP — R327 0ohms — R326 0ohms — PCI_CLKIN — PCI_CLK

+3.3VuP — U107 CY2305 (VDD REF CLKOUT GND CLK1 CLK2 CLK3 CLK4) — PCI_CLK — R78 0ohms — GND

R567 0ohms — CB1_CLK

DNP: R292 0ohms — PCIB_CLK; R565 0ohms — PCIB2_CLK; R566 0ohms — PCIB3_CLK

PCIA_CLK

+3.3V — ECO 580319

R349 should be 2.4K in order to overcome the internal pull-down on U14.AF23 (RSC_IN)

SHEET 1 — ARBITER_SEL

DNP R347 10Kohms, R348 10Kohms, R349 10Kohms

CARDTYPE_SEL ARBITER_SEL HOST_SEL

SW8 SPST4 — R358 121ohms — R359 121ohms — R360 121ohms

USE CONFIG DNP

0: CardBus
1: Mini-PCI

0: Mercury Host
1: Mercury Client

GND

PCIA_AD — SHEET 13,14
PCIA_CTRL — SHEET 13,14
PCIB_CTRL — SHEET 15
PCIB_AD — SHEET 15

RN31 PCIA_AD(6) PCIA_AD(4) PCIA_AD(2) PCIA_AD(0) PCIA_AD(7) PCIA_AD(5) PCIA_AD(3) PCIA_AD(1)

RN28 PCIA_AD(13) PCIA_AD(11) PCIA_AD(9) PCIA_CBE(0) PCIA_AD(14) PCIA_AD(12) PCIA_AD(10) PCIA_AD(8)

RN22 PCIA_TRDY~ PCIA_STOP~ PCIA_SERR~ PCIA_DEVSEL~ PCIA_PERR~ PCIA_AD(15) PCIA_CBE(1)

RN20 PCIA_AD(20) PCIA_AD(17) PCIA_PAR PCIA_AD(18) PCIA_CBE(2) PCIA_AD(16) PCIA_IRDY~ PCIA_FRAME~

RN17 PCIA_CBE(3) PCIA_AD(23) PCIA_AD(26) PCIA_AD(21) PCIA_AD(24) PCIA_AD(19) PCIA_AD(22) PCIA_IDSEL

RN14 PCIA_REQ1~ PCIA_AD(31) PCIA_AD(29) PCIA_GNT1~ PCIA_AD(27) PCIA_AD(25) PCIA_AD(30) PCIA_AD(28)

RN11 PCIA_GNT2~ PCIA_REQ2~ PCIA_GNT3~ PCIA_REQ3~ PCIA_INTB~ PCIA_INTA~ PCIA_RESET~ PCIA_INTC~

RN32 PCIA_INTD~ ARBITERA_SEL HOSTA_SEL CARDTYPEA_SEL

DNP RN80 PCIB_AD(6) PCIB_AD(4) PCIB_AD(2) PCIB_AD(0) PCIB_AD(7) PCIB_AD(5) PCIB_AD(3) PCIB_AD(1)

RN79 PCIB_AD(13) PCIB_AD(11) PCIB_AD(9) PCIB_CBE(0) PCIB_AD(14) PCIB_AD(12) PCIB_AD(10) PCIB_AD(8)

RN75 PCIB_TRDY~ PCIB_STOP~ PCIB_SERR~ PCIB_DEVSEL~ PCIB_PERR~ PCIB_AD(15) PCIB_CBE(1)

RN72 PCIB_AD(20) PCIB_AD(17) PCIB_PAR PCIB_AD(18) PCIB_CBE(2) PCIB_AD(16) PCIB_IRDY~ PCIB_FRAME~

RN70 PCIB_CBE(3) PCIB_AD(23) PCIB_AD(26) PCIB_AD(21) PCIB_AD(24) PCIB_AD(19) PCIB_AD(22) PCIB_IDSEL

RN68 PCIB_REQ1~ PCIB_AD(31) PCIB_AD(29) PCIB_GNT1~ PCIB_AD(27) PCIB_AD(25) PCIB_AD(30) PCIB_AD(28)

RN67 PCIB_GNT2~ PCIB_REQ2~ PCIB_GNT3~ PCIB_REQ3~ PCIB_INTB~ PCIB_INTA~ PCIB_RESET~ PCIB_INTC~

RN81 PCIB_INTD~ ARBITER_SEL HOST_SEL CARDTYPE_SEL

DNP 0ohms

PCIB_IDSEL — DNP TP9 TEST POINT

NOTE 1: CGNT# and CFRAME# pull-ups are located on PC Card per Cardbus spec.

NOTE 2: IDSEL not supported by Cardbus.

NOTE 3: PCI does not require GNT# or REQ# to be pulled up on host, but will be in this application. Cardbus requires a host pull-up on both GNT# and REQ#. The dev board is host only in CardBus mode and therefore does not require a GNT#/REQ# signal, however it will be populated here for test.

NOTE 4: INTA# used only as it is open drain at the driver and can be wire-or'd. An alternate method is to connect INTA# from Cardbus connector to INTC on the motherboard. Multifunction is relevant only to adapter card and the PCI slot can support a multifunction card with two interrupts.

NOTE 5: Power Management is not supported by the NS9750. PME# and 3.3Vaux pins are to be left floating per Power Management Spec.

NOTE 6: PCI oscillator at PCI_CLK_IN is a population option and is not required if using the internal system clock.

NOTE 7: CLKIN has internal weak pull-up.

NOTE 8: IDSEL tied to AD(11) if internal arbiter used and/or NS9750 as PCI Host, tied to AD[12] if external arbiter used and/or NS9750 as PCI Device. Test point included for other IDSEL/AD configurations.

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	1 App. note				
A	580124	Release				

APPROVALS	DATE
DESIGNED JZ	09/30/2005
DRAWN JZ	09/30/2005
CHECKED	09/30/2005
ENGINEER JZ	09/30/2005
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TITLE: NS9750 - PCI

SIZE	PART NO.	REV
D	30006011-01	C

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M ini-PCI

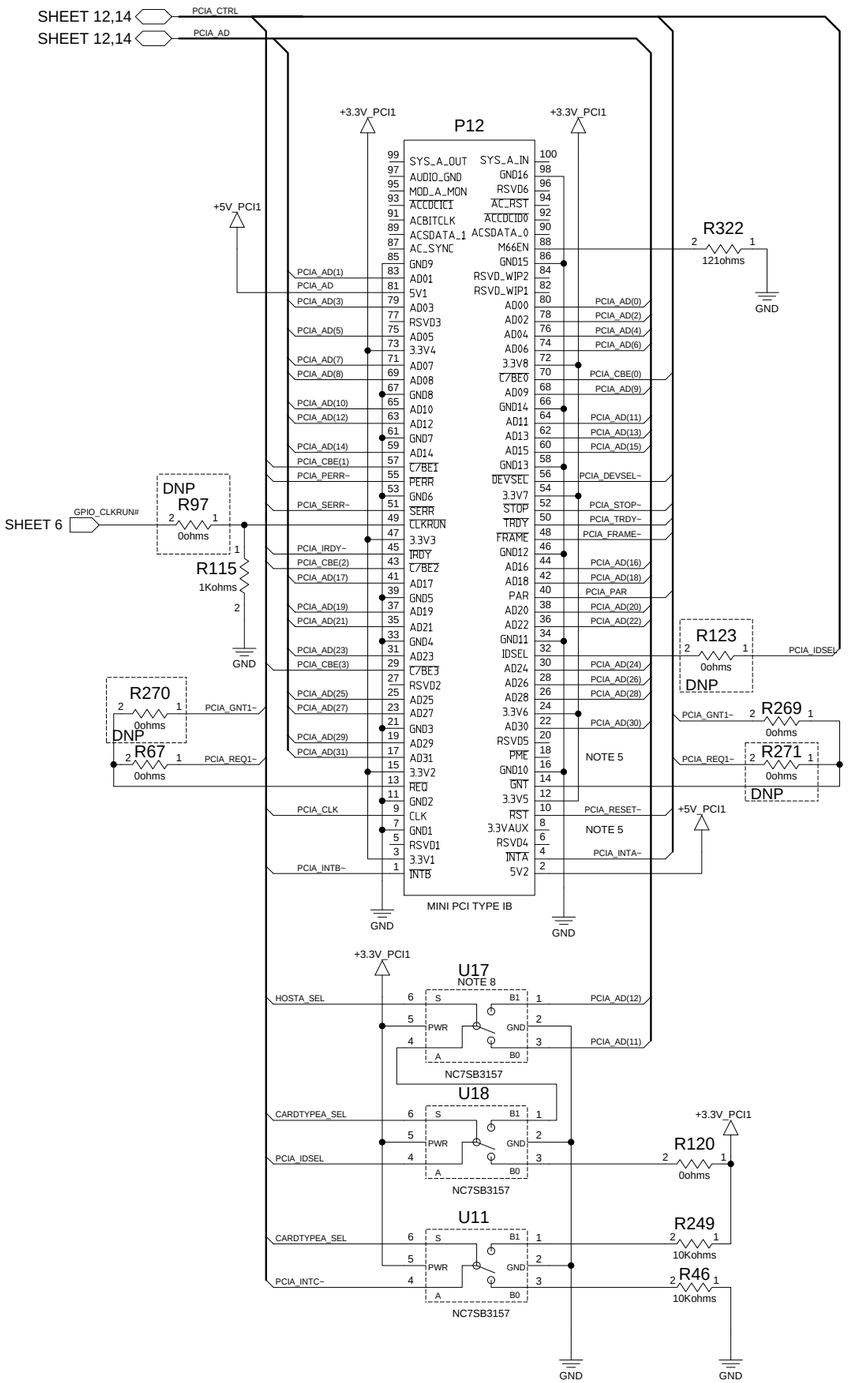
ECO 580319

Table of Contents

ECO 580319

PCB Stack up

1) Top Components
2) GND Plane 1
3) Signal 1
4) Signal 2
5) Power Plane
6) GND Plane 2
7) Signal 3
8) Signal 4
9) GND Plane 3
10) Bottom Components



Mini-PCI HOST
Populate R67 and R269
Depopulate R270 and R271
SW10 position 1 OFF
SW10 position 5 OFF
SW8 position 1 OFF
SW8 position 3 ON

Mini-PCI DEVICE
Must change connector
PCIA_CLK needs to route to PCI_CLKIN
Example: Depop R78, R326 wire R78 pin1 to R327 pin 2
Populate R270 and R271
Depopulate R67 and R269
SW10 position 1 ON
SW10 position 5 OFF
SW8 position 1 OFF
SW8 position 3 OFF

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	2 App. notes				
A	580124	Release				

APPROVALS	DATE
DESIGNED JZ	09/30/2005
DRAWN JZ	09/30/2005
CHECKED	09/30/2005
ENGINEER JZ	09/30/2005
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DO NOT SCALE DRAWING	

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TITLE: NS9750 - Mini PCI

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 13 of 18

30006011-01 REV C

32 Bit CardBus

P13 — CARDBUS68

34	GND2	GND4	68
33	CCLKRUN~	CCD2	67
32	RSVD1	CAD31	66
31	CAD29	CAD30	65
30	CAD27	CAD28	64
29	CAD26	CSTSCHG	63
28	CAD25	CAUDIO	62
27	CAD24	CBE3	61
26	CAD23	CREQ	60
25	CAD22	CSERR	59
24	CAD21	CRST	58
23	CAD20	CVS2	57
22	CAD18	CAD19	56
21	CCBE2	CAD17	55
20	CIRDY	CFRAME	54
19	CCLK	CTRDY	53
18	VPP1	VPP2	52
17	VCC1	VCC2	51
16	CINT	CDEVSEL	50
15	CGNT	CSTOP	49
14	CPERR	CBLOCK	48
13	CPAR	RSVD3	47
12	CCBE1	CAD16	46
11	CAD14	CAD15	45
10	CAD12	CAD13	44
9	CAD11	CVS1	43
8	CAD9	CAD10	42
7	CCBE0	CAD8	41
6	CAD7	RSVD2	40
5	CAD5	CAD6	39
4	CAD3	CAD4	38
3	CAD1	CAD2	37
2	CAD0	CCI	36
1	GND1	GND3	35

NC: pin 32 (CB_AD(29)), pin 31 (CB_AD(27)), pin 30 (CB_AD(26)), pin 29 (CB_AD(25)), pin 28 (CB_AD(24)), pin 27 (CB_AD(23)), pin 26 (CB_AD(22)), pin 25 (CB_AD(21)), pin 24 (CB_AD(20)), pin 23 (CB_AD(18)), pin 22 (CB_CBE(2)), pin 21 (CB_IRDY~), pin 20 (CB_CLK), pin 62, pin 47, pin 40

NOTE 1: CB_INTA~, CB_GNT1~, CB_PERR~, CB_PAR, CB_CBE(1), CB_AD(14), CB_AD(12), CB_AD(11), CB_AD(9), CB_AD(8), CB_AD(7), CB_AD(5), CB_AD(3), CB_AD(1), CB_AD(0)

CB_CCLKRUN~ → R268 10Kohms → +3.3V_PCI2; CB_CCLKRUN~ → R267 0ohms DNP → GND

CB_CCD1~ → R258 10Kohms → +3.3V_PCI1; CB_CCD2~ → R246 10Kohms → GND

CB_CLK → R291 75ohms → DNP; R290 75ohms → GND

Termination to be placed at end of CB_CLK trace.

CB_VPP, +3.3V_PCI2 → R303 10Kohms → CB_DEVSEL~

HOT SWAP BYPASS OPTION

R247	0ohms	PCIA_REQ3~	CB_CCD2~
R48	0ohms	PCIA_INTC~	CB_CSTSCHG
R55	0ohms	PCIA_RESET~	CB_RESET~
R56	1Kohms	PCIA_GNT3~	CB_CVS2
R57	1Kohms	PCIA_GNT2~	CB_CVS1
R58	0ohms	PCIA_REQ2~	CB_CCD1~
R68	0ohms	PCIA_INTB~	CB_CCLKRUN~

RN12 (0ohms)

1	O1	O16	16
PCIA_AD(31) 2	O2	O15	15 CB_AD(31)
PCIA_AD(30) 3	O3	O14	14 CB_AD(30)
PCIA_AD(29) 4	O4	O13	13 CB_AD(29)
PCIA_AD(28) 5	O5	O12	12 CB_AD(28)
PCIA_AD(27) 6	O6	O11	11 CB_AD(27)
PCIA_AD(26) 7	O7	O10	10 CB_AD(26)
PCIA_AD(25) 8	O8	O9	9 CB_AD(25)

RN15 (0ohms)

PCIA_CBE(3) 1	O1	O16	16 CB_CBE(3)
PCIA_AD(24) 2	O2	O15	15 CB_AD(24)
PCIA_REQ1~ 3	O3	O14	14 CB_REQ1~
PCIA_AD(23) 4	O4	O13	13 CB_AD(23)
PCIA_SERR~ 5	O5	O12	12 CB_SERR~
PCIA_AD(22) 6	O6	O11	11 CB_AD(22)
PCIA_AD(21) 7	O7	O10	10 CB_AD(21)
PCIA_AD(20) 8	O8	O9	9 CB_AD(20)

R85 0ohms: CB1_CLK → CB_CLK

RN18 (0ohms)

PCIA_AD(19) 1	O1	O16	16 CB_AD(19)
PCIA_AD(18) 2	O2	O15	15 CB_AD(18)
PCIA_AD(17) 3	O3	O14	14 CB_AD(17)
PCIA_CBE(2) 4	O4	O13	13 CB_CBE(2)
PCIA_FRAME~ 5	O5	O12	12 CB_FRAME~
PCIA_IRDY~ 6	O6	O11	11 CB_IRDY~
PCIA_TRDY~ 7	O7	O10	10 CB_TRDY~
PCIA_DEVSEL~ 8	O8	O9	9 CB_DEVSEL~

RN23 (0ohms)

PCIA_INTA~ 1	O1	O16	16 CB_INTA~
PCIA_STOP~ 2	O2	O15	15 CB_STOP~
PCIA_GNT1~ 3	O3	O14	14 CB_GNT1~
PCIA_PERR~ 4	O4	O13	13 CB_PERR~
PCIA_PAR 5	O5	O12	12 CB_PAR
PCIA_AD(16) 6	O6	O11	11 CB_AD(16)
PCIA_CBE(1) 7	O7	O10	10 CB_CBE(1)
PCIA_AD(15) 8	O8	O9	9 CB_AD(15)

RN26 (0ohms)

PCIA_AD(14) 1	O1	O16	16 CB_AD(14)
PCIA_AD(13) 2	O2	O15	15 CB_AD(13)
PCIA_AD(12) 3	O3	O14	14 CB_AD(12)
PCIA_AD(11) 4	O4	O13	13 CB_AD(11)
PCIA_AD(10) 5	O5	O12	12 CB_AD(10)
PCIA_AD(9) 6	O6	O11	11 CB_AD(9)
PCIA_AD(8) 7	O7	O10	10 CB_AD(8)
PCIA_CBE(0) 8	O8	O9	9 CB_CBE(0)

RN29 (0ohms)

PCIA_AD(7) 1	O1	O16	16 CB_AD(7)
PCIA_AD(6) 2	O2	O15	15 CB_AD(6)
PCIA_AD(5) 3	O3	O14	14 CB_AD(5)
PCIA_AD(4) 4	O4	O13	13 CB_AD(4)
PCIA_AD(3) 5	O5	O12	12 CB_AD(3)
PCIA_AD(2) 6	O6	O11	11 CB_AD(2)
PCIA_AD(1) 7	O7	O10	10 CB_AD(1)
PCIA_AD(0) 8	O8	O9	9 CB_AD(0)

HOT SWAP OPTION

DNP: R248 0ohms (CB_CSTSCHG); R99 0ohms (CB_CVS2); R305 0ohms (CB_CVS1)

U56 (DNP) — CBT3245A

PCIA_REQ2~	2 A1	B1 18	CB_CCD1~
PCIA_GNT2~	3 A2	B2 17	CB_CVS1
PCIA_GNT3~	4 A3	B3 16	CB_CVS2
PCIA_RESET~	5 A4	B4 15	CB_RESET~
PCIA_INTC~	6 A5	B5 14	CB_CSTSCHG
PCIA_REQ3~	7 A6	B6 13	CB_CCD2~
CARDTYPEA_SEL	8 A7	B7 12	CB_CCLKRUN~
	9 A8	B8 11	
	19 OE	GND 10	

R62 75ohms (CB_CCD1~); R61 75ohms (CB_CVS1); R60 75ohms (CB_CVS2); R59 75ohms (CB_RESET~); R49 75ohms (CB_CSTSCHG); R266 75ohms (CB_CCD2~); R69 75ohms (CB_CCLKRUN~)

R47 0ohms; R250 0ohms

U58 — CBT3245A

PCIA_INTB~	2 A1	B1 18	
PCIA_AD(25)	3 A2	B2 17	CB_AD(25)
PCIA_AD(26)	4 A3	B3 16	CB_AD(26)
PCIA_AD(27)	5 A4	B4 15	CB_AD(27)
PCIA_AD(28)	6 A5	B5 14	CB_AD(28)
PCIA_AD(29)	7 A6	B6 13	CB_AD(29)
PCIA_AD(30)	8 A7	B7 12	CB_AD(30)
PCIA_AD(31)	9 A8	B8 11	CB_AD(31)
CB_HOT	19 OE	GND 10	

RN13 (0ohms)

1	O1	O16	16
CB_AD(25) 2	O2	O15	15 CB_AD(26)
CB_AD(27) 3	O3	O14	14 CB_AD(28)
CB_AD(29) 4	O4	O13	13 CB_AD(30)
CB_AD(31) 5	O5	O12	12 CB_HOT
CB_AD(25) 6	O6	O11	11 CB_AD(27)
CB_AD(26) 7	O7	O10	10 CB_AD(28)
CB_AD(29) 8	O8	O9	9 CB_AD(30)

U59 — CBT3245A

PCIA_AD(20)	2 A1	B1 18	CB_AD(20)
PCIA_AD(21)	3 A2	B2 17	CB_AD(21)
PCIA_AD(22)	4 A3	B3 16	CB_AD(22)
PCIA_SERR~	5 A4	B4 15	CB_SERR~
PCIA_AD(23)	6 A5	B5 14	CB_AD(23)
PCIA_REQ1~	7 A6	B6 13	CB_REQ1~
PCIA_AD(24)	8 A7	B7 12	CB_AD(24)
PCIA_CBE(3)	9 A8	B8 11	CB_CBE(3)
	19 OE	GND 10	

RN16 (0ohms)

1	O1	O16	16
CB_AD(20) 2	O2	O15	15 CB_AD(21)
CB_AD(22) 3	O3	O14	14 CB_SERR~
CB_AD(23) 4	O4	O13	13 CB_REQ1~
CB_AD(24) 5	O5	O12	12 CB_AD(3)
CB_AD(20) 6	O6	O11	11 CB_AD(21)
CB_AD(21) 7	O7	O10	10 CB_AD(22)
CB_AD(22) 8	O8	O9	9 CB_AD(23)

U62 — CBT3245A

PCIA_DEVSEL~	2 A1	B1 18	CB_DEVSEL~
PCIA_TRDY~	3 A2	B2 17	CB_TRDY~
PCIA_IRDY~	4 A3	B3 16	CB_IRDY~
PCIA_FRAME~	5 A4	B4 15	CB_FRAME~
PCIA_CBE(2)	6 A5	B5 14	CB_CBE(2)
PCIA_AD(17)	7 A6	B6 13	CB_AD(17)
PCIA_AD(18)	8 A7	B7 12	CB_AD(18)
PCIA_AD(19)	9 A8	B8 11	CB_AD(19)
	19 OE	GND 10	

RN19 (0ohms)

1	O1	O16	16
CB_DEVSEL~ 2	O2	O15	15 CB_TRDY~
CB_IRDY~ 3	O3	O14	14 CB_FRAME~
CB_CBE(2) 4	O4	O13	13 CB_AD(17)
CB_AD(18) 5	O5	O12	12 CB_AD(19)
CB_AD(16) 6	O6	O11	11 CB_PERR~
CB_GNT1~ 7	O7	O10	10 CB_STOP~
CB_INTA~ 8	O8	O9	9

U66 — CBT3245A

PCIA_AD(15)	2 A1	B1 18	CB_AD(15)
PCIA_CBE(1)	3 A2	B2 17	CB_CBE(1)
PCIA_AD(16)	4 A3	B3 16	CB_AD(16)
PCIA_PAR	5 A4	B4 15	CB_PAR
PCIA_PERR~	6 A5	B5 14	CB_PERR~
PCIA_GNT1~	7 A6	B6 13	CB_GNT1~
PCIA_STOP~	8 A7	B7 12	CB_STOP~
PCIA_INTA~	9 A8	B8 11	CB_INTA~
	19 OE	GND 10	

RN24 (0ohms)

1	O1	O16	16
CB_AD(15) 2	O2	O15	15 CB_CBE(1)
CB_AD(16) 3	O3	O14	14 CB_PAR
CB_PERR~ 4	O4	O13	13 CB_GNT1~
CB_STOP~ 5	O5	O12	12 CB_INTA~
CB_AD(15) 6	O6	O11	11 CB_CBE(1)
CB_AD(1) 7	O7	O10	10 CB_AD(2)
CB_AD(3) 8	O8	O9	9

U69 — CBT3245A

PCIA_CBE(0)	2 A1	B1 18	CB_CBE(0)
PCIA_AD(8)	3 A2	B2 17	CB_AD(8)
PCIA_AD(9)	4 A3	B3 16	CB_AD(9)
PCIA_AD(10)	5 A4	B4 15	CB_AD(10)
PCIA_AD(11)	6 A5	B5 14	CB_AD(11)
PCIA_AD(12)	7 A6	B6 13	CB_AD(12)
PCIA_AD(13)	8 A7	B7 12	CB_AD(13)
PCIA_AD(14)	9 A8	B8 11	CB_AD(14)
	19 OE	GND 10	

RN27 (0ohms)

1	O1	O16	16
CB_AD(8) 2	O2	O15	15 CB_AD(9)
CB_AD(10) 3	O3	O14	14 CB_AD(11)
CB_AD(12) 4	O4	O13	13 CB_AD(13)
CB_AD(14) 5	O5	O12	12 CB_CBE(0)
CB_AD(8) 6	O6	O11	11 CB_AD(9)
CB_AD(9) 7	O7	O10	10 CB_AD(10)
CB_AD(11) 8	O8	O9	9 CB_AD(12)

U70 — CBT3245A

PCIA_AD(0)	2 A1	B1 18	CB_AD(0)
PCIA_AD(1)	3 A2	B2 17	CB_AD(1)
PCIA_AD(2)	4 A3	B3 16	CB_AD(2)
PCIA_AD(3)	5 A4	B4 15	CB_AD(3)
PCIA_AD(4)	6 A5	B5 14	CB_AD(4)
PCIA_AD(5)	7 A6	B6 13	CB_AD(5)
PCIA_AD(6)	8 A7	B7 12	CB_AD(6)
PCIA_AD(7)	9 A8	B8 11	CB_AD(7)
	19 OE	GND 10	

RN30 (0ohms)

1	O1	O16	16
CB_AD(0) 2	O2	O15	15 CB_AD(1)
CB_AD(2) 3	O3	O14	14 CB_AD(3)
CB_AD(4) 4	O4	O13	13 CB_AD(5)
CB_AD(6) 5	O5	O12	12 CB_AD(7)
CB_AD(0) 6	O6	O11	11 CB_AD(1)
CB_AD(1) 7	O7	O10	10 CB_AD(2)
CB_AD(3) 8	O8	O9	9 CB_AD(4)

U15 — NC7SB3157: S, B1, PWR, GND, A, B0; CB1_CLK → CB_CLK

R304 0ohms (CB_CLK)

HOT SWAP OPTION

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	No changes				
A	580124	Release				

APPROVALS		DATE
DESIGNED	JZ	09/30/2005
DRAWN	JZ	09/30/2005
CHECKED		09/30/2005
ENGINEER	JZ	09/30/2005
02:27:27 PM		
DO NOT SCALE DRAWING		

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TITLE: NS9750 - PCI CARDBUS/BUFFERS

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 14 of 18

30006011-01 REV C

SHEET 12 PCIB_CTRL
SHEET 12 PCIB_AD

P48 DNP — PCI SOCKET 3.3V — 3.3 VOLT SLOT 1
P47 DNP — PCI SOCKET 3.3V — 3.3 VOLT SLOT 2
P46 — PCI SOCKET 3.3V — 3.3 VOLT SLOT 3

R35 4.7Kohms
R53 10Kohms DNP
R54 10Kohms
GPIO_S1_PRS1~
GPIO_S1_PRS2~

R34 4.7Kohms
R44 4.7Kohms
R45 4.7Kohms
R63 10Kohms DNP
R65 10Kohms
R37 4.7Kohms
GPIO_S2_PRS1
GPIO_S2_PRS2~

R36 4.7Kohms
R50 4.7Kohms
R51 4.7Kohms
R64 10Kohms
R66 10Kohms
R571 75ohms DNP
R570 75ohms
PCIB2_CLK
This port will not support dynamic PRS.
Termination to be placed at end of PCIB2_CLK trace.

R40 4.7Kohms
GPIO_S3_PRS1~
GPIO_S3_PRS2~

R38 4.7Kohms
R39 4.7Kohms
R52 4.7Kohms
R70 121ohms
R71 121ohms
PCIB3_CLK
Termination to be placed at end of PCIB3_CLK trace.

R569 75ohms DNP
R568 75ohms
PCIB_CLK
Termination to be placed at end of PCIB_CLK trace.

R321 10Kohms DNP

Slot one only has IDSEL option to AD11 to test Master functionality on standard slots.
R324 0ohms
R107 0ohms DNP
TP8 TEST POINT

R323 10Kohms DNP
R98 10Kohms
R102 10Kohms

R108 0ohms
R100 10Kohms
R101 10Kohms
R105 10Kohms DNP

R109 0ohms
R103 10Kohms
R104 10Kohms

R131 10Kohms
R130 10Kohms
R133 10Kohms
R132 10Kohms
R135 10Kohms
R134 10Kohms

GND

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	No changes				
A	580124	Release				

APPROVALS	DATE
DESIGNED JZ	09/30/2005
DRAWN JZ	09/30/2005
CHECKED	09/30/2005
ENGINEER JZ	09/30/2005
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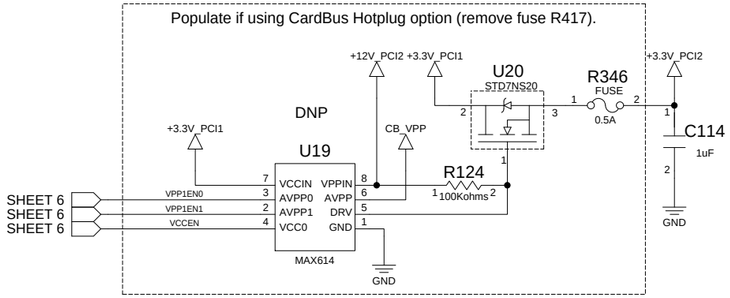
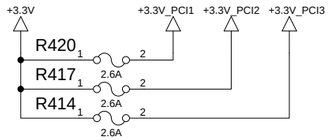
TITLE: NS9750 - Full PCI Slots

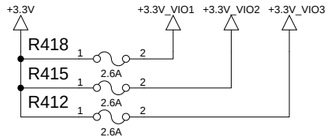
SIZE	PART NO.	REV
D	30006011-01	C

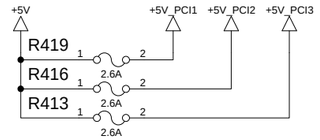
SCALE: NTS | VERIBEST | SHEET 15 of 18

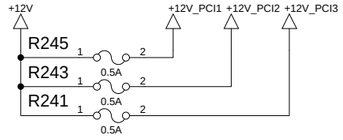
Populate if using CardBus Hotplug option (remove fuse R417).

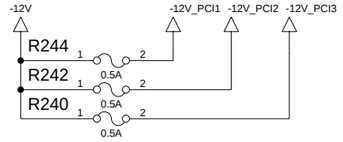


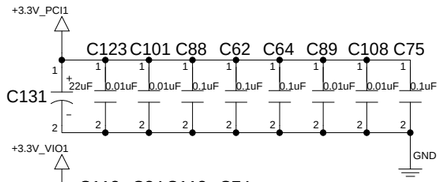


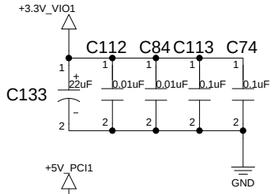


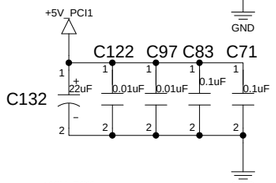


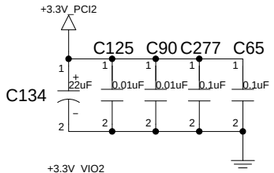


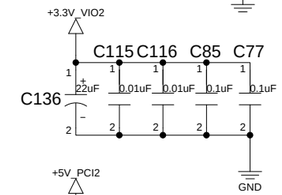


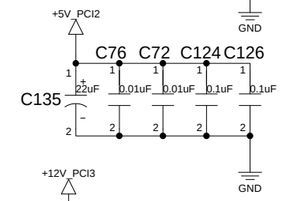


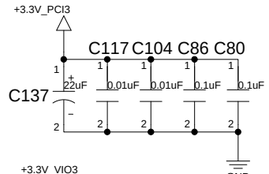


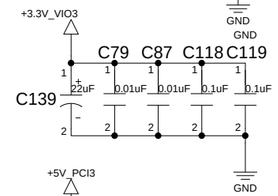


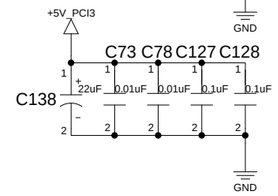


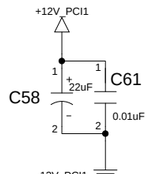


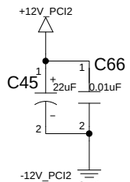












REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	No changes				
A	580124	Release				

APPROVALS	DATE
DESIGNED JZ	09/30/2005
DRAWN JZ	09/30/2005
CHECKED	09/30/2005
ENGINEER JZ	09/30/2005
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DO NOT SCALE DRAWING	

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TITLE: NS9750 - PCI fuses, Decoupling

SIZE	PART NO.	REV
D	30006011-01	C

SCALE: NTS | VERIBEST | SHEET 16 of 18

40 PIN MII CONNECTOR

30006011-01 REV C

P6

DB40

MII_SHIELD

L19

ETHBUS

RN76

RN78

RN74

R601 0ohms

R602 0ohms

R32 0ohms

R31 0ohms

R603 0ohms

R96 0ohms

R91 0ohms

R317 0ohms

R92 0ohms

R318 0ohms

R316 0ohms

R309 0ohms

R90 0ohms

R302 0ohms

R77 0ohms

R301 0ohms

R76 0ohms

R308 0ohms

R84 0ohms

R83 0ohms

R95 0ohms

R328 0ohms

R300 0ohms

R75 0ohms

R331 0ohms

DNP

GND

+5V

+3.3V

C93 0.1uF

R80 0ohms

U13 INH OUT

C99 18pF

C100 18pF

X1 25

R93 0ohms

R94 0ohms

R89 47ohms

R88 0ohms

TP10 TEST POINT

TP11 TEST POINT

U65 BCM5221KPT

XTALI XTALO REF_CLK

TXD0 TXD1 TXD2 TXD3 TX_EN TX_ER TX_CLK

RXD0 RXD1 RXD2 RXD3 RX_DV RX_ER RX_CLK

COL CRS MDC MDIO RESET

AD0/FDX_LED AD1/COL_LED AD2/ACT_LED AD3/PAUSE AD4

FDX SD+ SD- TESTEN MII_EN LOW_PWR ENERGY_DET

REGVDD REGAVDD DVDD1 DVDD2 AVDD1 AVDD2 BIASVDD OVDD1 OVDD2 OVDD/NC

TD+ TD- RD+ RD- RDAC

XMTLED/INTR/FDXLED JTAG_EN LNKLED/MEDIA_CONV/TDI RCVLED/MDIX_DIS/TDO SPDLED/ADV_PAUSE/TMS F100/TCK ANEN/TRST

DGND1 DGND2 DGND3 DGND4 AGND1 AGND2 BIASGND XTALGND

R82 47ohms

R81 47ohms

R74 1.5Kohms

R87 0ohms

R86 1.27Kohms

R72 4.7Kohms

ALL MAGENTA (solid box) present for RMII

B_ETH_RESET

SHEET 1

ETH_RESET

R332 0ohms DNP

R342 0ohms

R106 0ohms POP TO HOLD RMII PHY IN RESET

CLOCK TERMINATION USED HERE DUE TO DEV BOARD'S MANY FUNCTIONS - NORMALLY NOT NECESSARY

C391 0.01uF C390 0.01uF

R606 47ohms R605 47ohms

FOR TEST ONLY

U14 ETHERNET NS9750

P15 DNP MICTOR38

RN25 RN21 0ohms

R604 0ohms R600 0ohms R127 0ohms R129 0ohms R117 0ohms

I_ETH_RESET

R118 0ohms DNP

POP TO HOLD MII PHY IN RESET

C295 18pF C294 18pF

X4 25

R114 10Kohms R119 10Kohms

R128 1.5Kohms

TP12 TEST POINT

U16 LXT971ABGA 10/100 ETHERNET CONTROLER

R333 22.1Kohms

R112 0ohms R111 0ohms

C106 0.01uF C296 0.1uF C299 0.1uF

R125 51.1ohms R344 51.1ohms

C300 0.1uF C107 0.01uF

C276 0.1uF C92 0.01uF C282 1uF

C283 0.001uF

R79 49.9ohms R310 49.9ohms

R319 49.9ohms R329 49.9ohms

C98 0.001uF

R320 150ohms R311 150ohms

R73 4.7Kohms

C94 CLOSE TO PIN 6 0.1uF

C91 0.1uF C96 0.1uF C269 0.001uF C103 0.001uF C95 0.1uF C121 0.1uF C102 10uF

P14 RJ45 8P W/MAGNETICS/LEDS

LEFT RIGHT

ETH_SHIELD L35 SHIELD SHIELD

L38

DEPOP FOR AUTO_NEG

R345 220ohms

R368 0ohms DNP

R367 0ohms

P17 RJ45 8P W/MAGNETICS/LEDS

R113 0ohms R110 0ohms DNP

C298 0.01uF C297 1uF

L11

R126 220ohms R334 220ohms

R366 220ohms DNP

C111 0.01uF C105 0.01uF C109 0.01uF

C110 270pF C120 270pF L37

REV	ECO	DESCRIPTION OF CHANGE	BY	CKD	APPR	DATE
C	580319	No changes				
A	580124	Release				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
02:27:27 PM	
DO NOT SCALE DRAWING	

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TITLE: NS9750 - Ethernet

SIZE	PART NO.	REV
D	30006011-01	C

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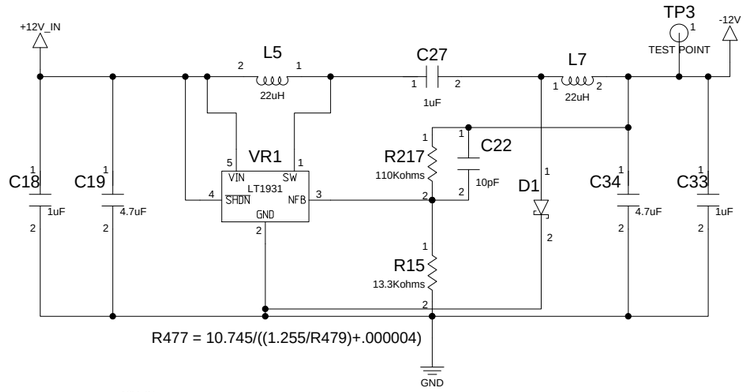
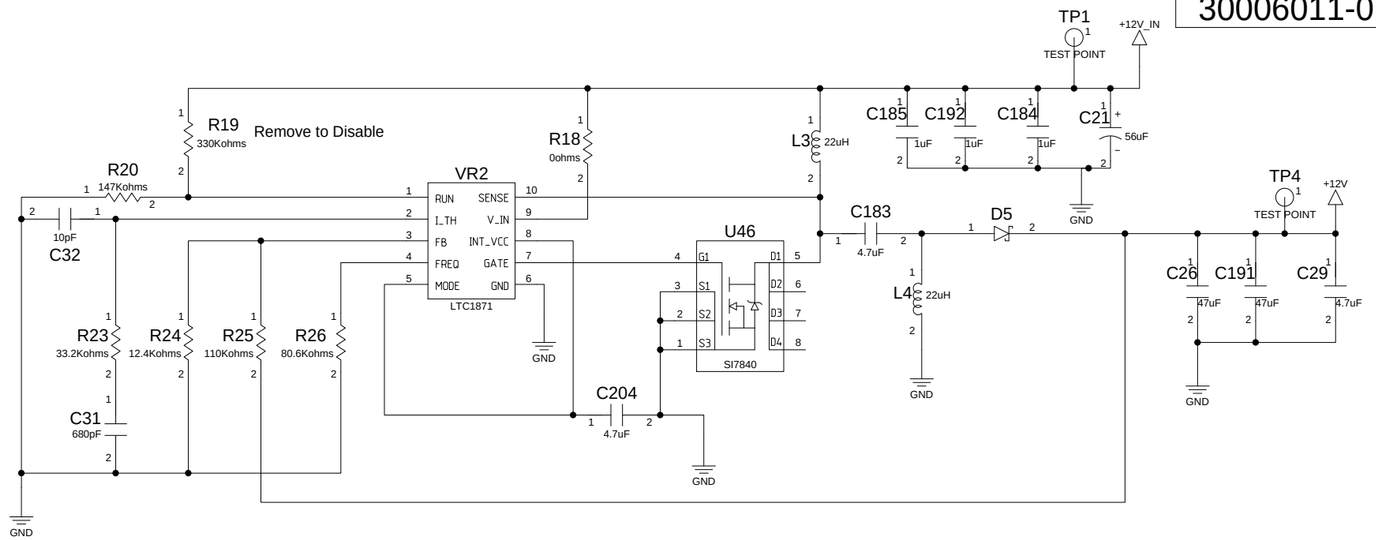
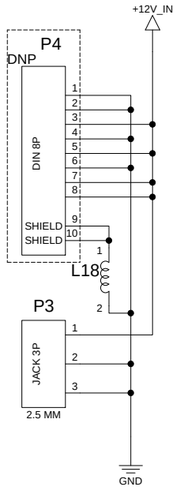
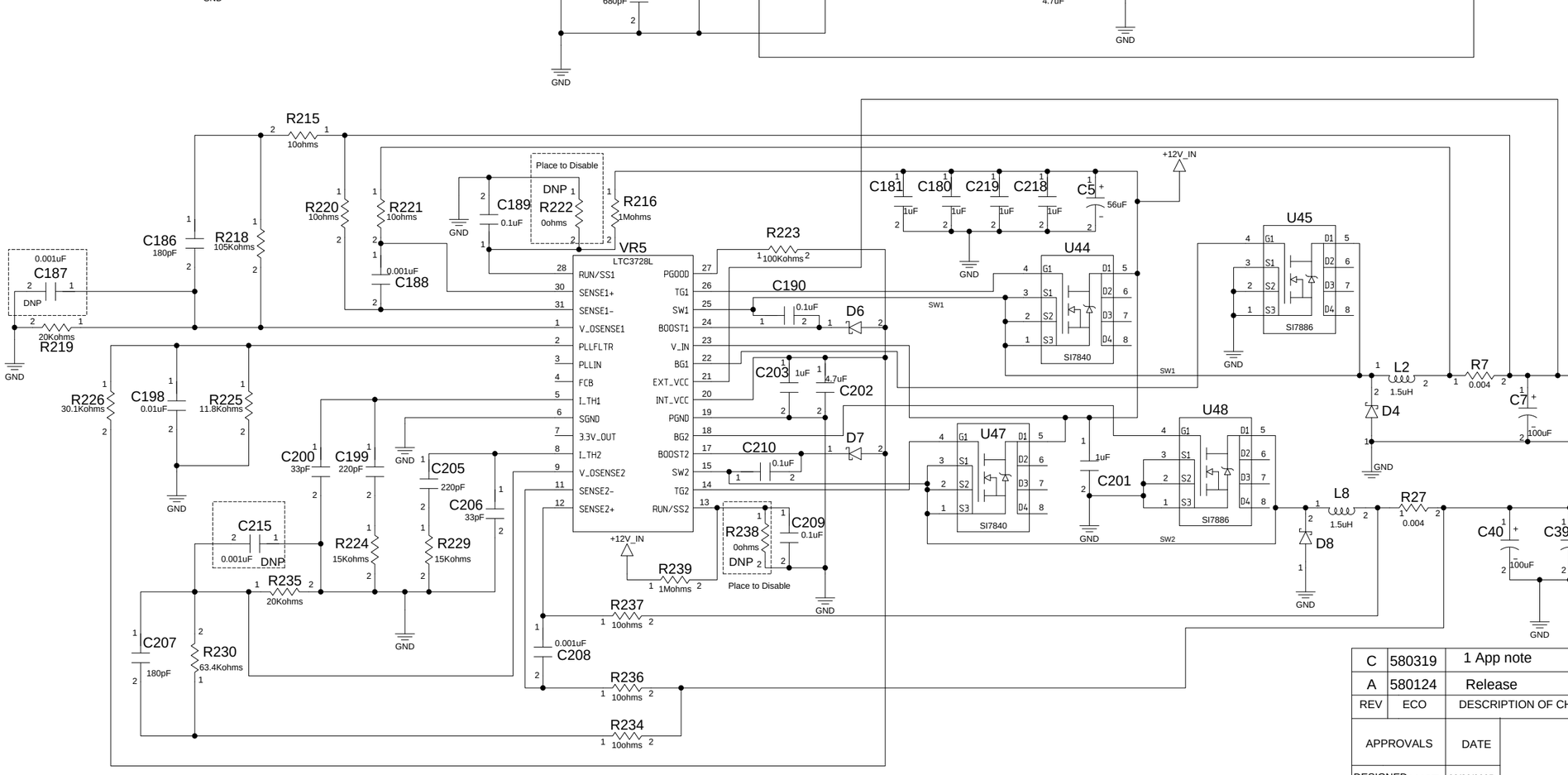
30006011-01 REV C









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C	580319	1 App note				
A	580124	Release				

APPROVALS	DATE
DESIGNED WJR	09/30/2005
DRAWN WJR	09/30/2005
CHECKED	09/30/2005
ENGINEER WJR	09/30/2005
02:27:27 PM	
DO NOT SCALE DRAWING	

Digi

TITLE: NS9750 -POWER

SIZE	PART NO.	REV
D	30006011-01	C

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ECO 580319
IMPORTANT Disclaimer!
This power supply design does not meet the latest NS9750 power sequencing requirement. See the NS9750B-A1 data sheet.