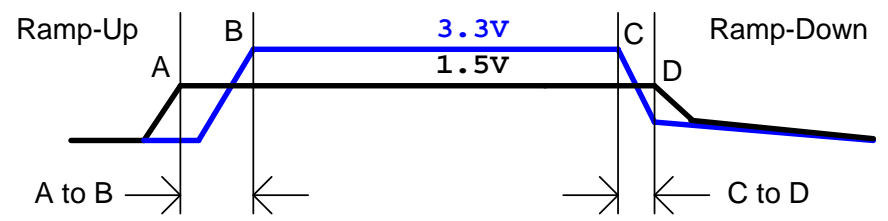


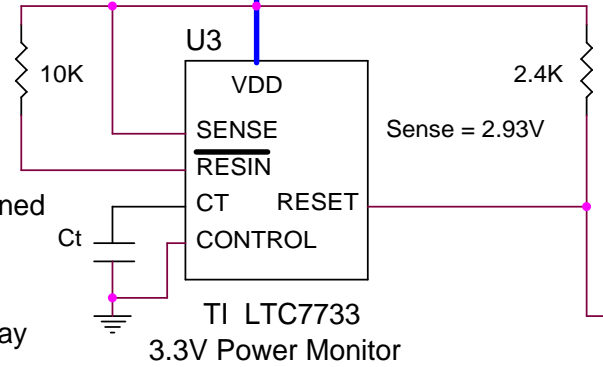
- A = 3.3V_IN at 2.0V
- B = 3.3V_IN at 2.93V + Td (RESET delay)
- C = 3.3V_IN at 2.93V
- D = 3.3V_IN at 2.0V



A to B = 1.5V at 80%, or above, precedes 3.3V at 80%, or above, by 1 -100 ms

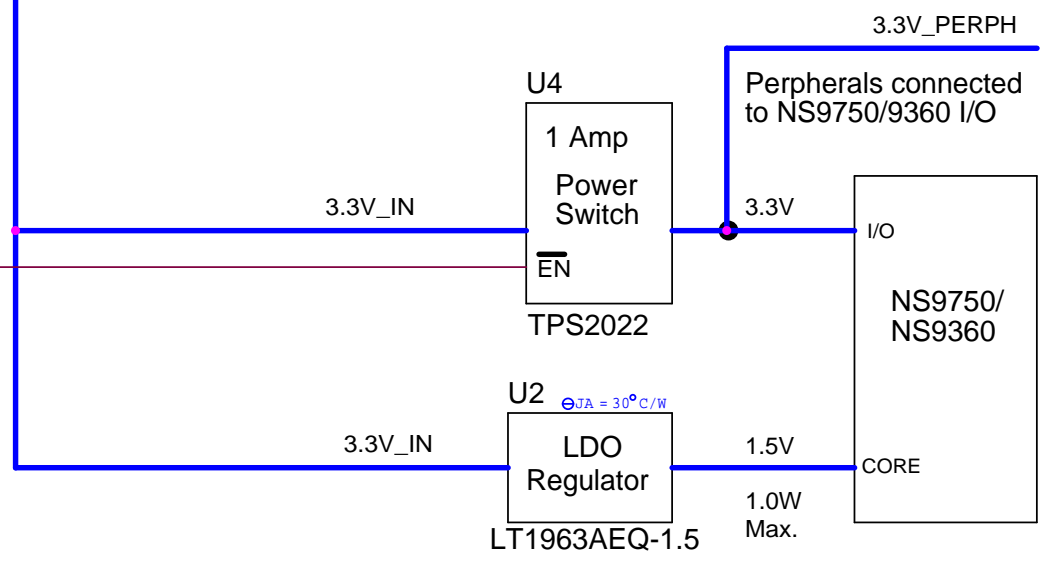
C to D = 1.5V maintained at 80%, or above, until 3.3V reaches 80% or below.

RESET delay is determined by capacitor on Ct.
 $T_d = 2.1 \times 10,000 \times C_t$
 $T_d = \text{sec.}; C_t = \text{farads}$
 $C_t = 0.22\mu\text{F} = 4.6\text{ms delay}$



Power Up:
 3.3V I/O is held off by monitor so that 1.5V core comes up first.

Power Down:
 Monitor turns off 3.3V I/O before 1.5V drops.



NS9750/9360 Power Sequencing Block Diagram - 5V or 3V source