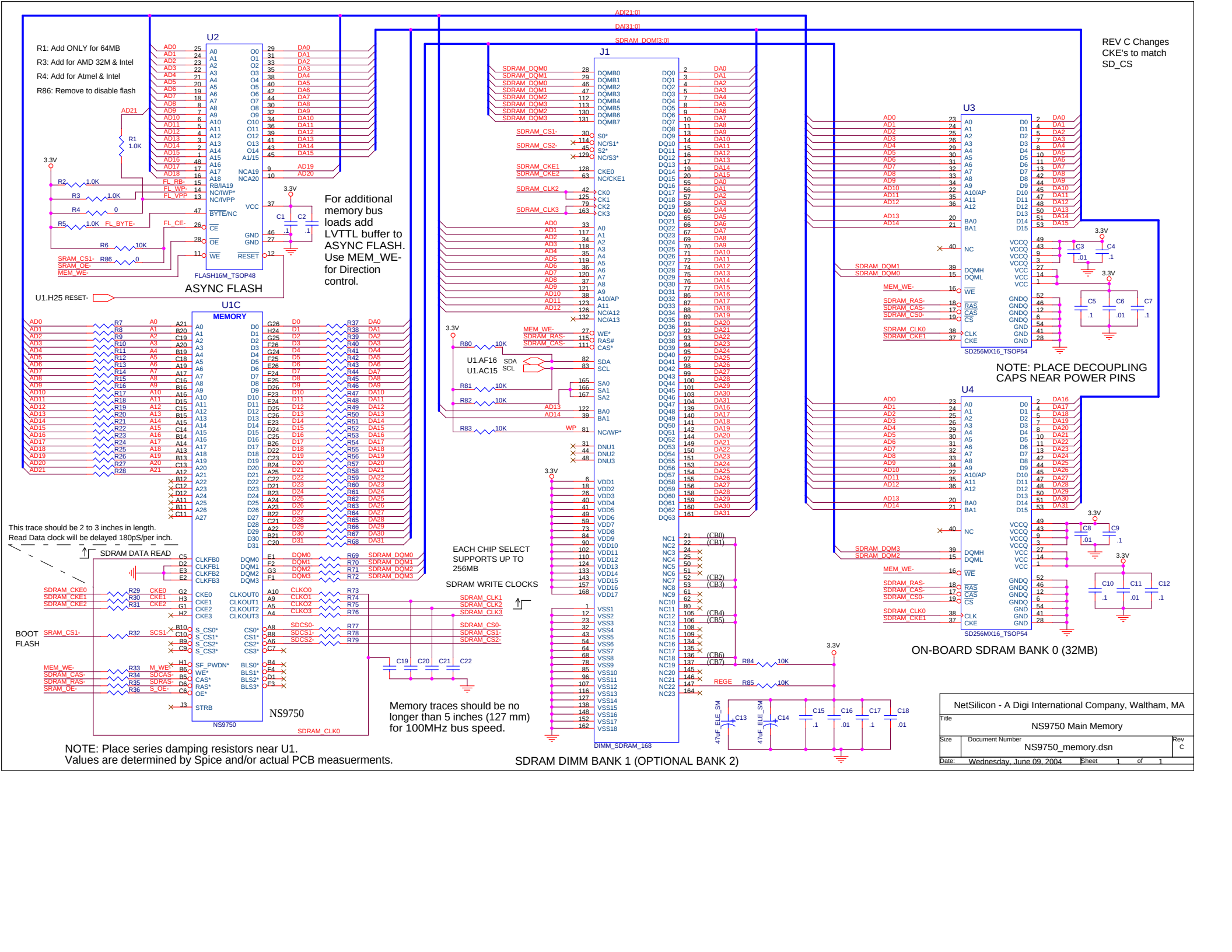
R1: Add ONLY for 64MB
R3: Add for AMD 32M & Intel
R4: Add for Atmel & Intel
R86: Remove to disable flash
REV C Changes
CKE's to match
SD_CS
U2
FLASH16M_TSOP48
ASYNC FLASH
For additional memory bus loads add LVTTL buffer to ASYNC FLASH. Use MEM_WE- for Direction control.
U1C
MEMORY
NS9750
SDRAM DATA READ
This trace should be 2 to 3 inches in length.
Read Data clock will be delayed 180pS/per inch.
BOOT FLASH
EACH CHIP SELECT SUPPORTS UP TO 256MB
SDRAM WRITE CLOCKS
Memory traces should be no longer than 5 inches (127 mm) for 100MHz bus speed.
J1
DIMM_SDRAM_168
SDRAM DIMM BANK 1 (OPTIONAL BANK 2)
U3
U4
SD256MX16_TSOP54
NOTE: PLACE DECOUPLING CAPS NEAR POWER PINS
ON-BOARD SDRAM BANK 0 (32MB)
NOTE: Place series damping resistors near U1.
Values are determined by Spice and/or actual PCB measuerments.
NetSilicon - A Digi International Company, Waltham, MA
Title
NS9750 Main Memory
Size
Document Number
NS9750_memory.dsn
Rev C
Date: Wednesday, June 09, 2004
Sheet 1 of 1