Rev	Drawn	Description of change(s)	Date
A	DEN	Initial Schematic	7/28/04
B	DEN	Changes after testing prototype boards	11/09/04
01	DJS	Text & Sh. size cleanup, R193 to NO_STUFF & Rev B to 01	11/09/04
01	DEN/DJS	Part description changes to correct package sizes	11/23/04
01	DJS	Added R79-10K Pull-up to PIRQ_N - Touch Screen Interrupt.	11/29/04
01	DJS	Routed CF_CD2_N through the CPLD for use with GPIO10	12/07/04
A	DJS	55001149-01 board changes - 27-dec-04 rework.doc (To -02)	01/03/05
A	DJS	Added JP4, SPI boot	01/10/05
A	DJS	Changed Compact Flash addressing	01/26/05
A	DJS	Changed cover page title block	02/18/05
B	DJS	Added Power Supply sequencing disclamer on sheet 12	06/21/05
C	DJS	Global Change - Cooper to NS9360; Added Bootstrap Table on Sheet 9	10/12/05
D	DJS	Updated Bootstrap Table on Sheet 9, and added Errata comments.	05/03/05

Table of Contents:

REF SCH 30006401-02 REV D
USE BOM 55001149-02

NetSilicon - A Digi International Co.

Title: NS9360 Development Board

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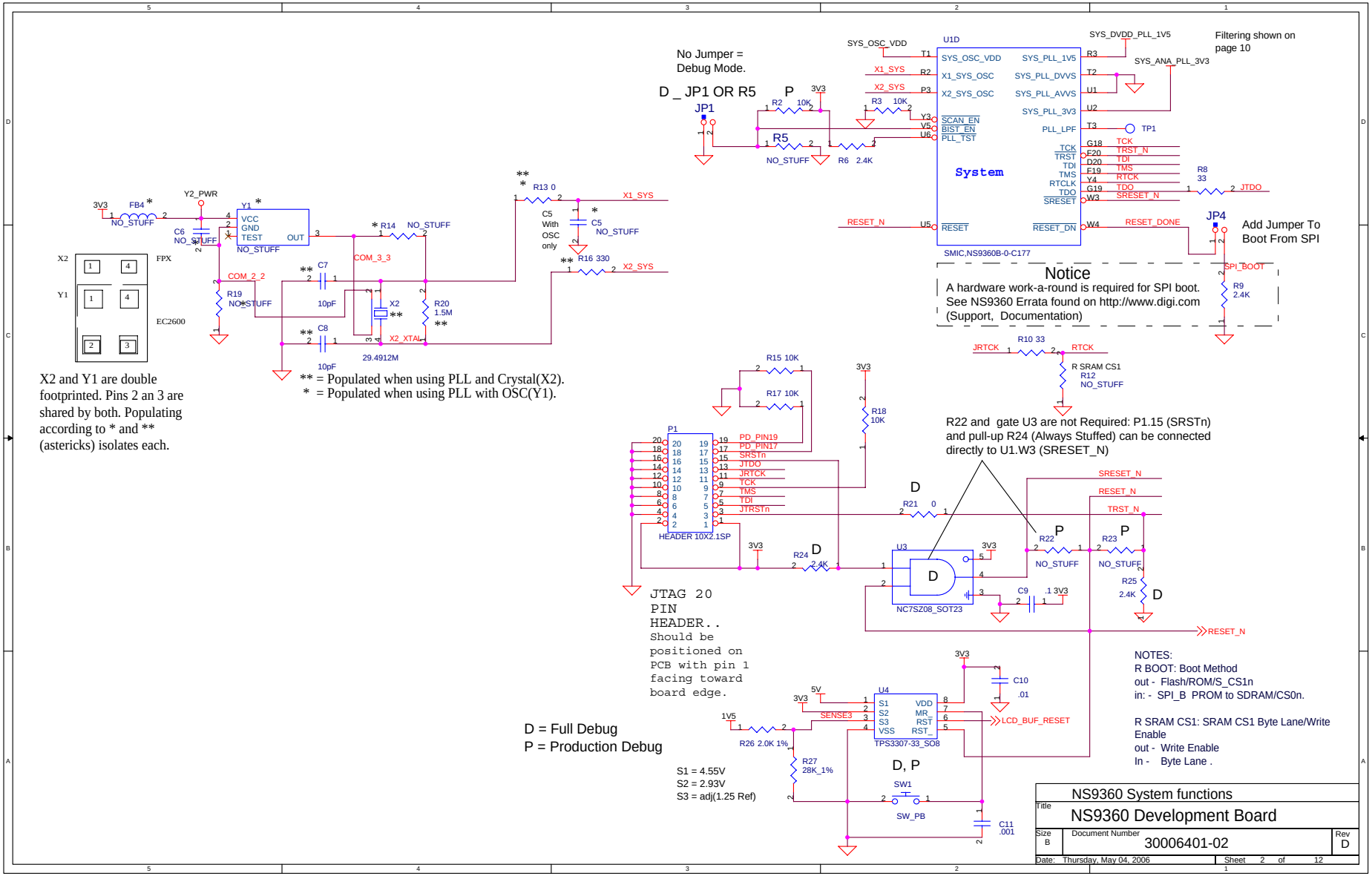
No Jumper = Debug Mode.
D _ JP1 OR R5
P
JP1
R5
NO_STUFF
R6 2.4K
R2 10K
R3 10K
3V3
U1D
SYS_OSC_VDD
X1_SYS
X2_SYS
SCAN_EN
BIST_EN
PLL_TST
SYS_PLL_1V5
SYS_PLL_DVVS
SYS_PLL_AVVS
SYS_PLL_3V3
PLL_LPF
SYS_DVDD_PLL_1V5
SYS_ANA_PLL_3V3
TP1
System
TCK
TRST
TDI
TMS
RTCLK
TDO
SRESET
RESET_N
RESET
RESET_DN
RESET_DONE
SMIC,NS9360B-0-C177
Filtering shown on page 10
JP4
Add Jumper To Boot From SPI
SPI_BOOT
R9 2.4K
R8 33
JTDO
Notice
A hardware work-a-round is required for SPI boot. See NS9360 Errata found on http://www.digi.com (Support, Documentation)
R10 33
JRTCK
RTCK
R SRAM CS1
R12
NO_STUFF
Y2_PWR
FB4
Y1
VCC
GND
TEST
OUT
C6
R14
R13 0
X1_SYS
C5
With OSC only
R16 330
X2_SYS
COM_3_3
COM_2_2
R19
C7
10pF
X2
R20 1.5M
X2_XTAL
C8
10pF
29.4912M
X2
Y1
FPX
EC2600
X2 and Y1 are double footprinted. Pins 2 an 3 are shared by both. Populating according to * and ** (astericks) isolates each.
** = Populated when using PLL and Crystal(X2).
* = Populated when using PLL with OSC(Y1).
R15 10K
R17 10K
R18 10K
P1
PD_PIN19
PD_PIN17
SRSTn
JTDO
JRTCK
TCK
TMS
TDI
JTRSTn
HEADER 10X2.1SP
JTAG 20 PIN HEADER.. Should be positioned on PCB with pin 1 facing toward board edge.
R22 and gate U3 are not Required: P1.15 (SRSTn) and pull-up R24 (Always Stuffed) can be connected directly to U1.W3 (SRESET_N)
R21 0
R22
R23
R24 2.4K
R25 2.4K
NO_STUFF
U3
NC7SZ08_SOT23
C9 .1
SRESET_N
RESET_N
TRST_N
D = Full Debug
P = Production Debug
U4
TPS3307-33_SO8
SENSE3
1V5
5V
R26 2.0K 1%
R27 28K_1%
C10 .01
C11 .001
LCD_BUF_RESET
S1 = 4.55V
S2 = 2.93V
S3 = adj(1.25 Ref)
D, P
SW1
SW_PB
NOTES:
R BOOT: Boot Method
out - Flash/ROM/S_CS1n
in: - SPI_B PROM to SDRAM/CS0n.
R SRAM CS1: SRAM CS1 Byte Lane/Write Enable
out - Write Enable
In - Byte Lane .
NS9360 System functions
Title
NS9360 Development Board
Size B
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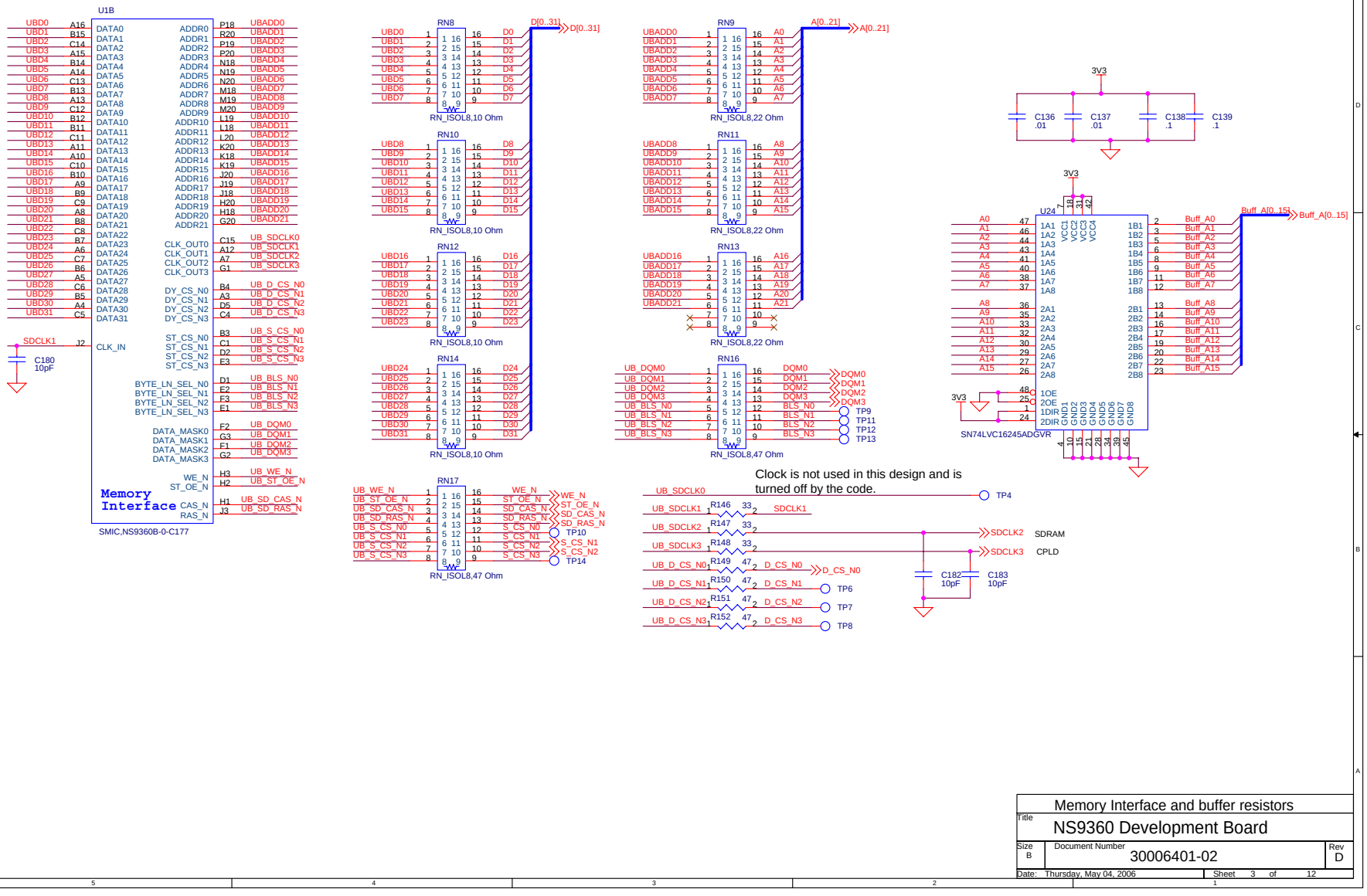
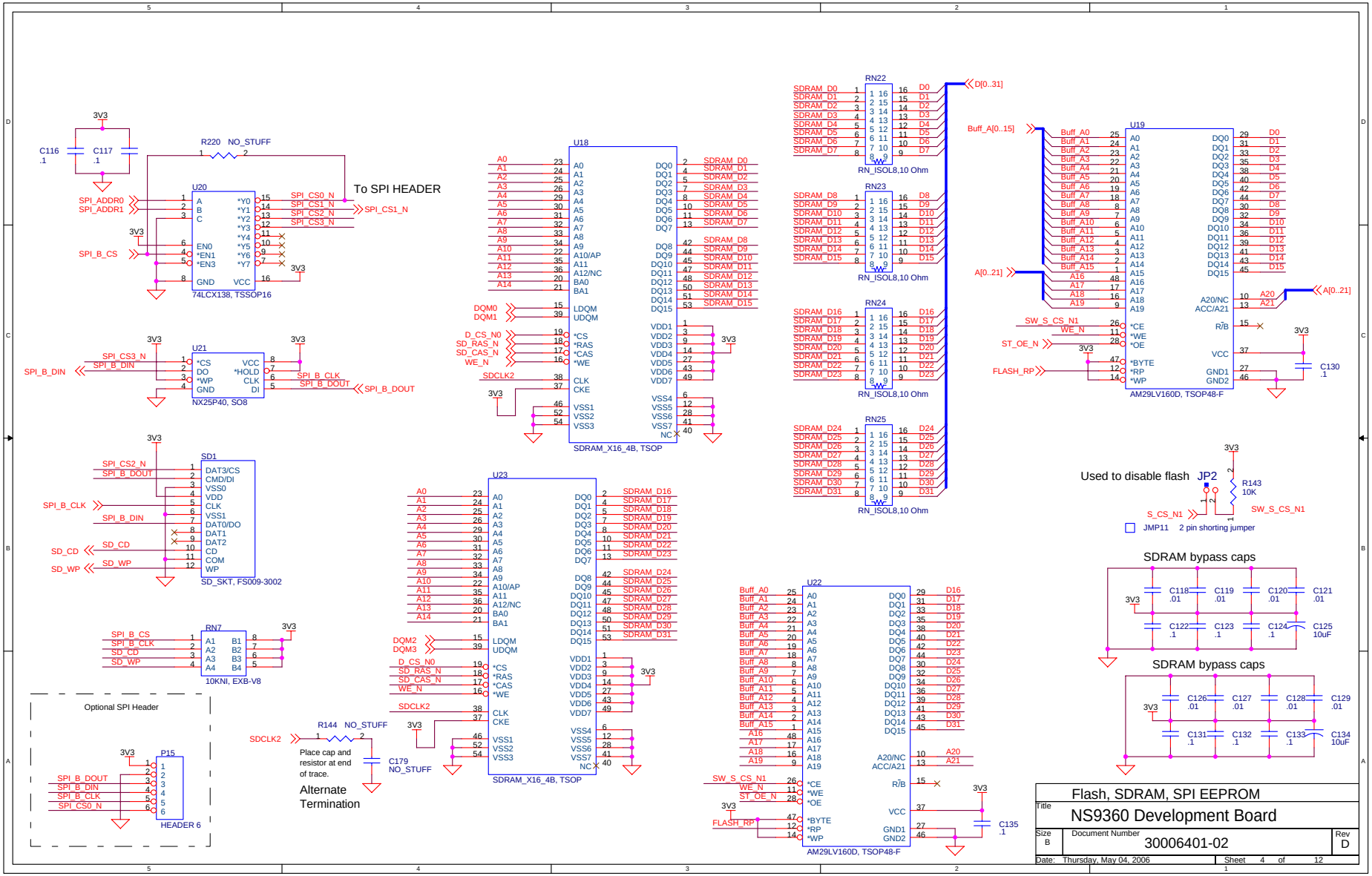

U1B
SMIC,NS9360B-0-C177
Memory Interface
RN8
RN9
RN10
RN11
RN12
RN13
RN14
RN16
RN17
RN_ISOL8,10 Ohm
RN_ISOL8,22 Ohm
RN_ISOL8,47 Ohm
Clock is not used in this design and is turned off by the code.
U24
SN74LVC16245ADGVR
C136 .01
C137 .01
C138 .1
C139 .1
C180 10pF
C182 10pF
C183 10pF
SDRAM
CPLD
Memory Interface and buffer resistors
NS9360 Development Board
30006401-02
Thursday, May 04, 2006
Sheet 3 of 12



Flash, SDRAM, SPI EEPROM

Title: NS9360 Development Board

Size	Document Number	Rev
B	30006401-02	D

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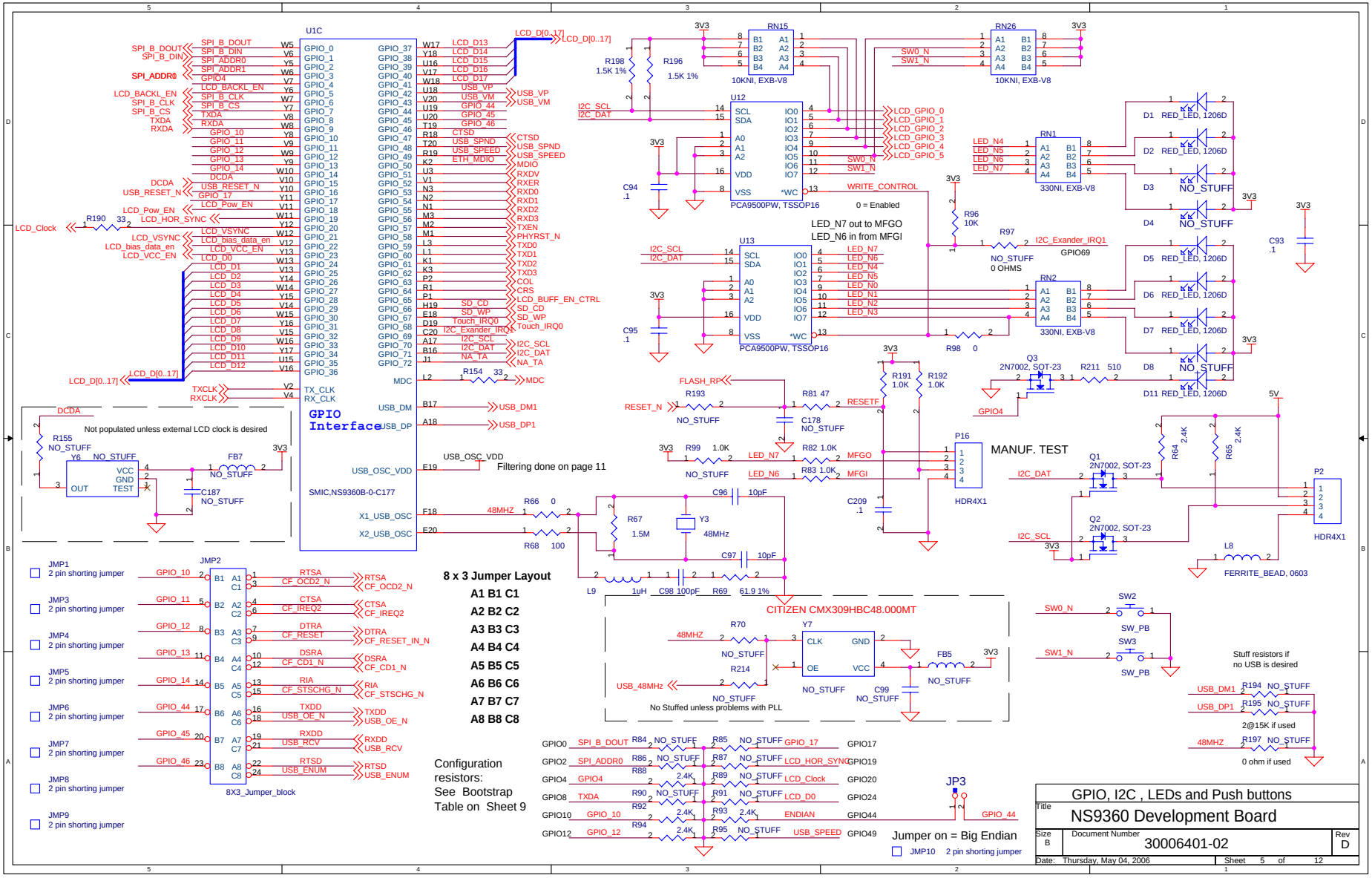
U1C
GPIO Interface
SMIC,NS9360B-0-C177
Not populated unless external LCD clock is desired
Filtering done on page 11
LED_N7 out to MFGO
LED_N6 in from MFGI
0 = Enabled
MANUF. TEST
CITIZEN CMX309HBC48.000MT
No Stuffed unless problems with PLL
8 x 3 Jumper Layout
A1 B1 C1
A2 B2 C2
A3 B3 C3
A4 B4 C4
A5 B5 C5
A6 B6 C6
A7 B7 C7
A8 B8 C8
Configuration resistors: See Bootstrap Table on Sheet 9
8X3_Jumper_block
Jumper on = Big Endian
JMP10 2 pin shorting jumper
Stuff resistors if no USB is desired
2@15K if used
0 ohm if used
GPIO, I2C , LEDs and Push buttons
NS9360 Development Board
30006401-02
Rev D
Thursday, May 04, 2006
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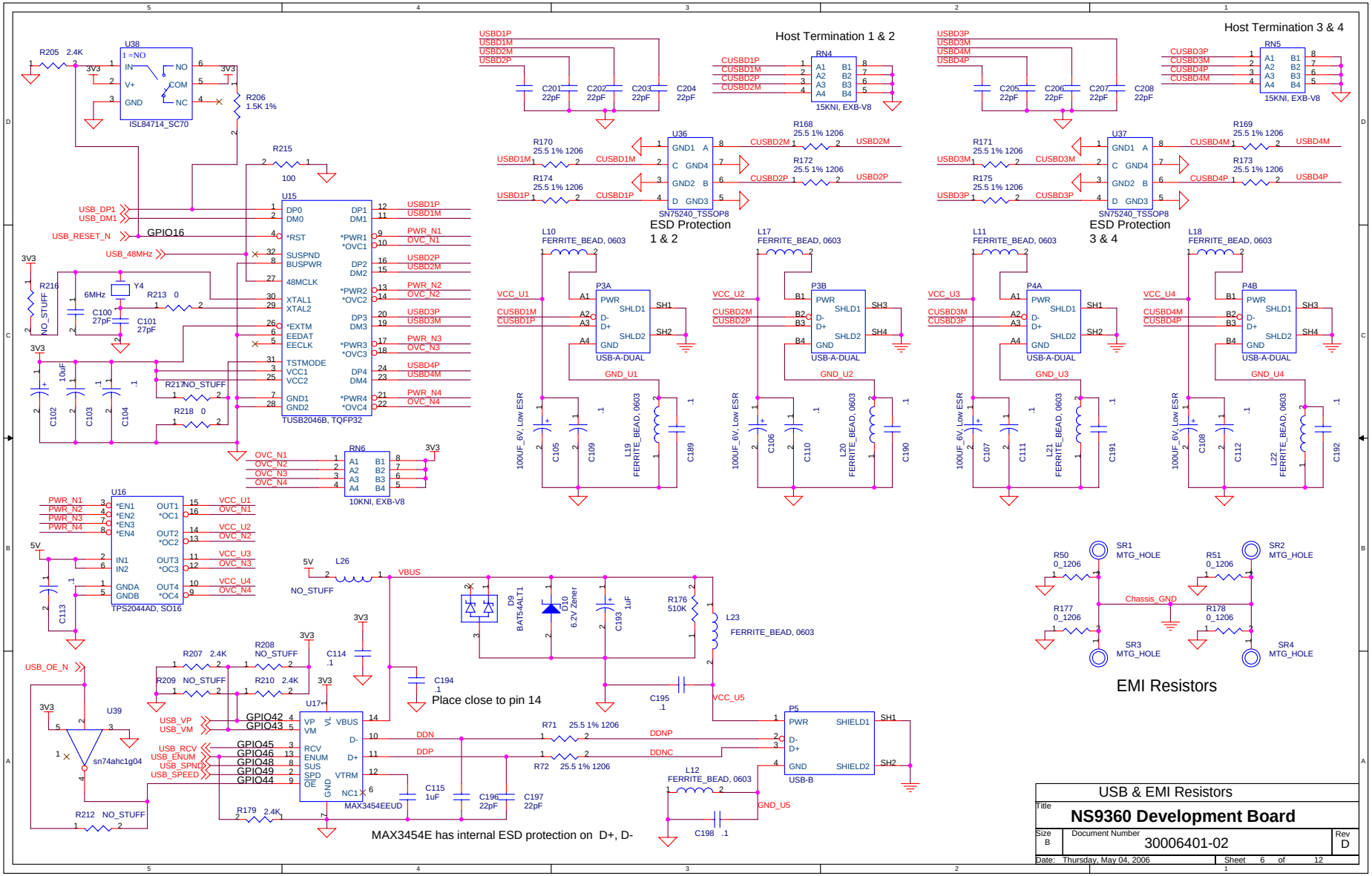
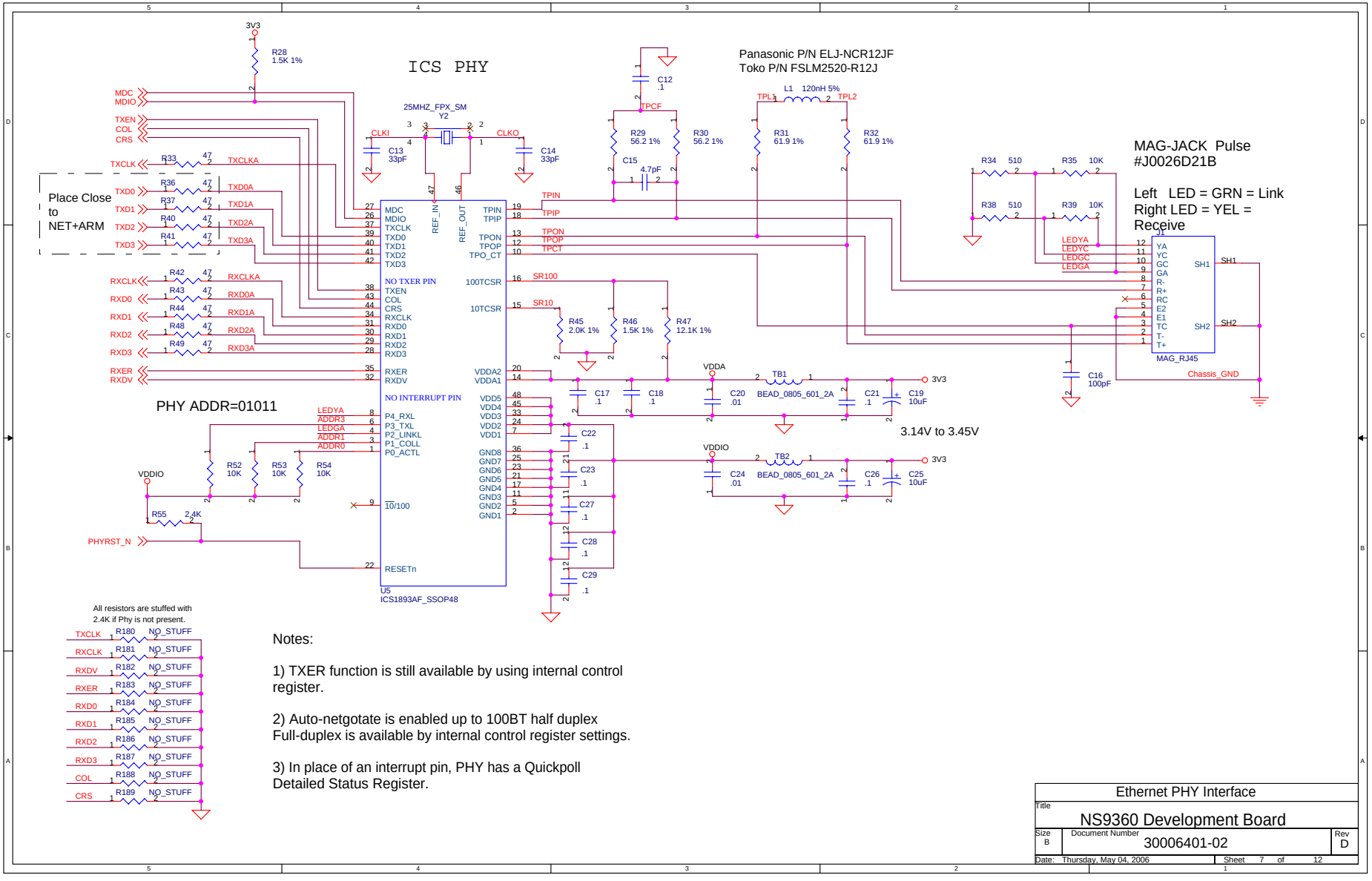

Host Termination 1 & 2
Host Termination 3 & 4
ESD Protection 1 & 2
ESD Protection 3 & 4
EMI Resistors
Place close to pin 14
MAX3454E has internal ESD protection on D+, D-
USB & EMI Resistors
NS9360 Development Board
30006401-02
Thursday, May 04, 2006
Sheet 6 of 12



Notes:

1) TXER function is still available by using internal control register.

2) Auto-netgotate is enabled up to 100BT half duplex
Full-duplex is available by internal control register settings.

3) In place of an interrupt pin, PHY has a Quickpoll Detailed Status Register.

Title	Ethernet PHY Interface
	NS9360 Development Board
Size B	Document Number 30006401-02
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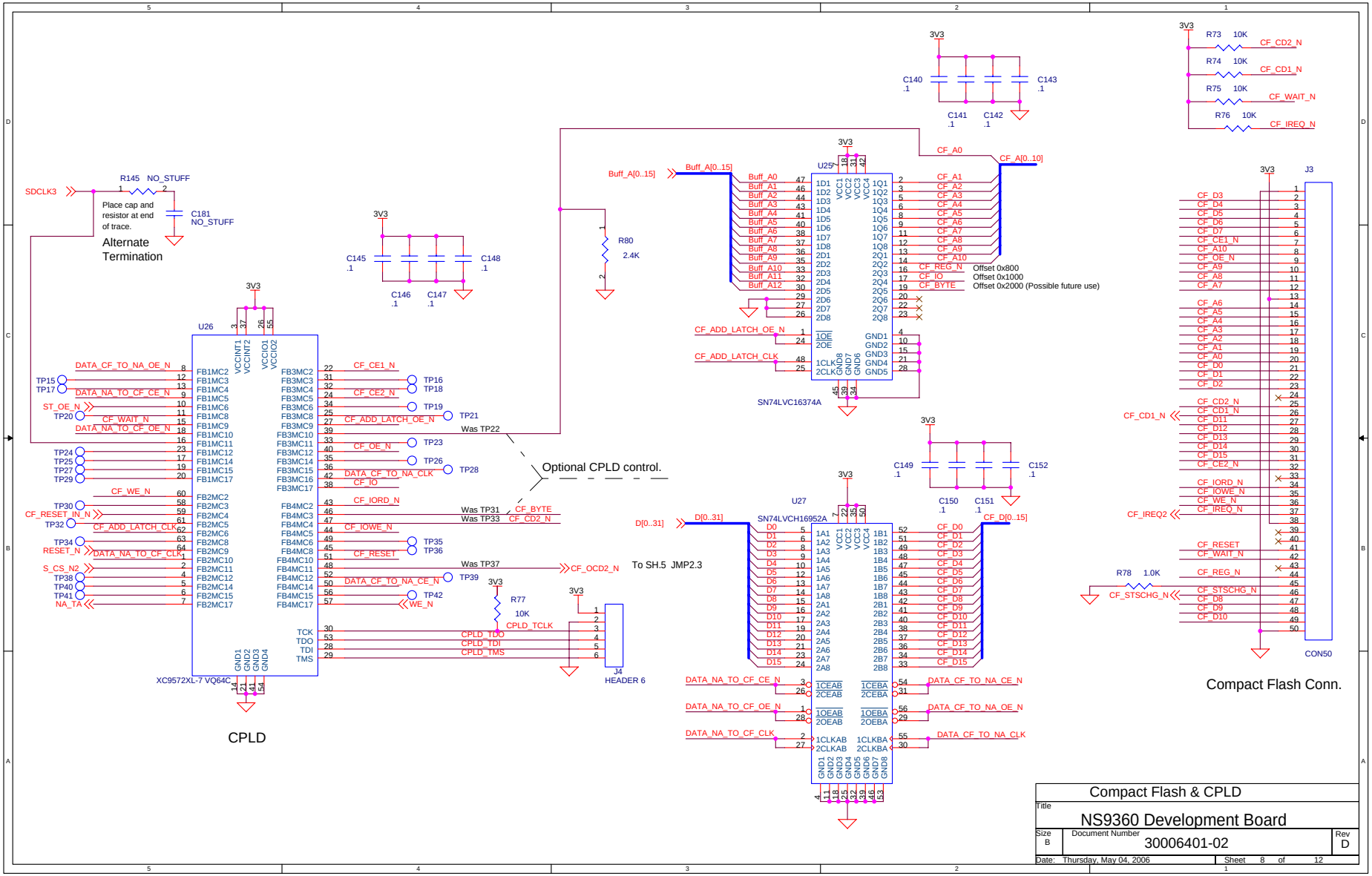
Compact Flash & CPLD
NS9360 Development Board
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Size B
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CPLD
Compact Flash Conn.
Optional CPLD control.
Alternate Termination
Place cap and resistor at end of trace.
SN74LVC16374A
SN74LVCH16952A
XC9572XL-7 VQ64C
HEADER 6
CON50
Offset 0x800
Offset 0x1000
Offset 0x2000 (Possible future use)
To SH.5 JMP2.3

NS9360 Bootstrap Table

IMPORTANT: All bootstrap inputs have an internal pull-up, and are latched (5) x1_sys_osc clock cycles after reset_n is deasserted (goes high)

rtck - byte_lane_sel_n[3:0] Static Chip select 1

rtck	PB	S_CS1 mode
1	0	Write Enable
0	1	Byte Lane Enable

No pull-down defaults to Write Enable (rtck into FS is inverted)

reset_done - Boot Up Mode

reset_done	BMM	Boot Up Mode
0	0	Boot from SPI on Serial port B
1	1	Boot from S_CS1 Flash/ROM

No pull-down boots from S_CS1 Flash/ROM

gpio[2],[0] - PLL FS[1:0] (PLL Frequency Select)

gpio	FS	Divide by
10	00	1
11	01	2
00	10	4
01	11	8

No pull-down defaults to Divide by 2 (gpio[2] into FS is inverted)

gpio[17],[12],[10],[8],[4] - PLL ND[4:0] (PLL Multiplier, ND+1).
Sample clock frequency setting with 29.4912 MHz input clock and FS/2

gpio	PLLND	ND+1	Frequency (MHz)
10010	10111	24	176.9472
10001	10100	21	154.8288
01000	01101	14	103.2192

gpio[10] and [4] into PLLND are inverted.
ND+1 of 24 = 176.9472MHz, pull-down GPIO[12], GPIO[10], GPIO[4]
ND+1 of 21 = 154.8288MHz, pull-down GPIO[12], GPIO[10], GPIO[8]
ND+1 of 14 = 103.2192MHz, pull-down GPIO[17], GPIO[10], GPIO[8], GPIO[4]
Note: No pull-downs = ND+1 of 27. This is out of range for the NS9360.

gpio[19] - Reserved.

gpio	PLLBP	Mode
0	0	PLL is bypassd
1	1	PLL Not bypassed

No pull-down enables the PLL (Should NEVER be pulled down during boot)

gpio[24],[20] - Static Chip select 1 data width

gpio	MW	Data Width
01	00	8 bits
00	01	16 bits
11	10	32 bits
10	11	Reserved

No pull-down defaults to x32 bit Flash/ROM (gpio[20] into MW is inverted)

gpio[44] - Endian Mode

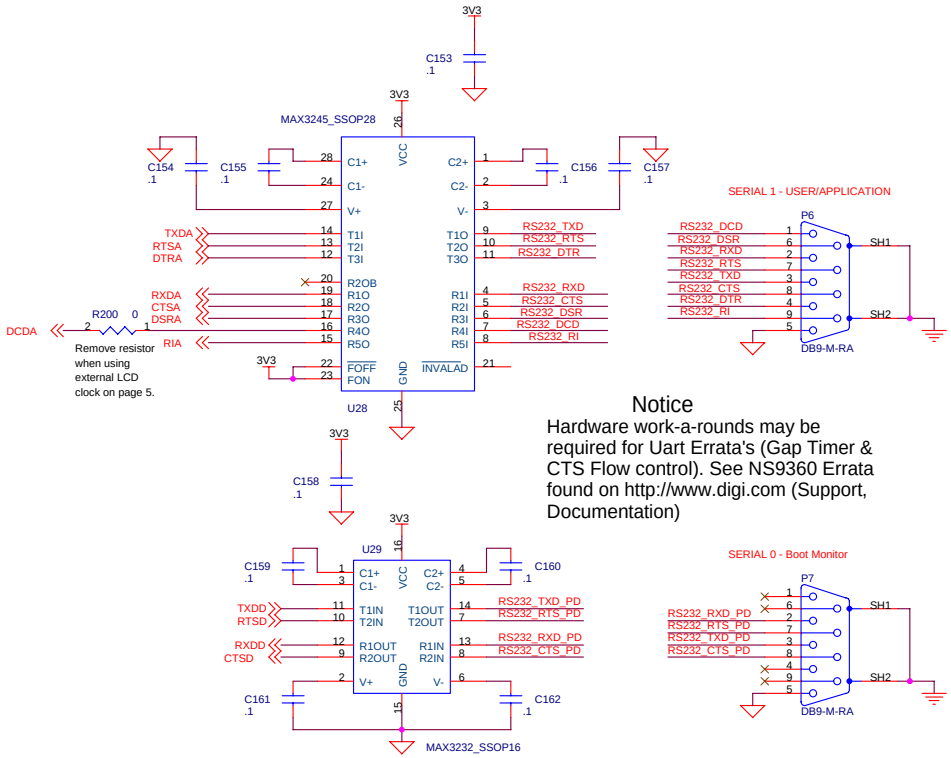
gpio	END	Mode
1	0	Little endian
0	1	Big endian

No pull-down defaults to Little endian (gpio[44] into END is inverted)

gpio[49] - Static Chip select 1 polarity

gpio	PC	S_CS1 polarity
1	0	Active low
0	1	Active high

No pull-down defaults to Active low (gpio[49] into PC is inverted)



Notice

Hardware work-a-rounds may be required for Uart Errata's (Gap Timer & CTS Flow control). See NS9360 Errata found on http://www.digi.com (Support, Documentation)

RS232 Outputs & Bootstrap Table

Title: NS9360 Development Board		
Size: B	Document Number: 30006401-02	Rev: D
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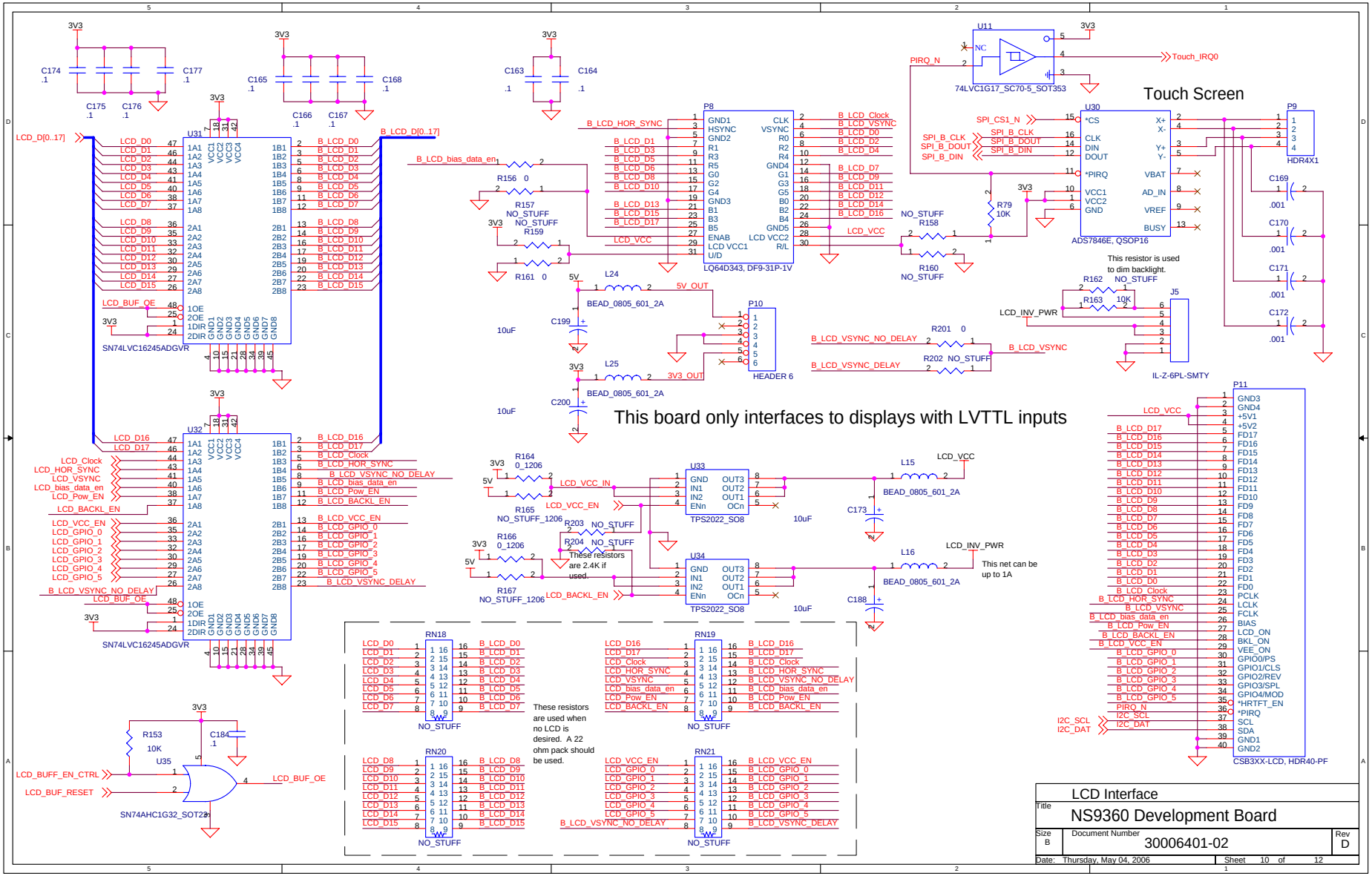
Touch Screen
This board only interfaces to displays with LVTTL inputs
These resistors are used when no LCD is desired. A 22 ohm pack should be used.
These resistors are 2.4K if used.
This net can be up to 1A
This resistor is used to dim backlight.
LCD Interface
NS9360 Development Board
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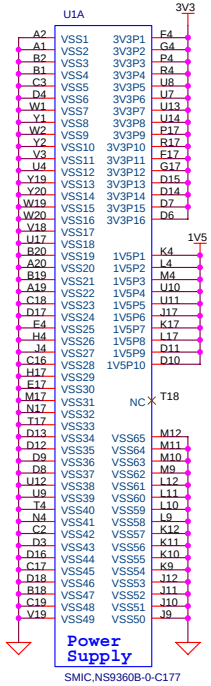
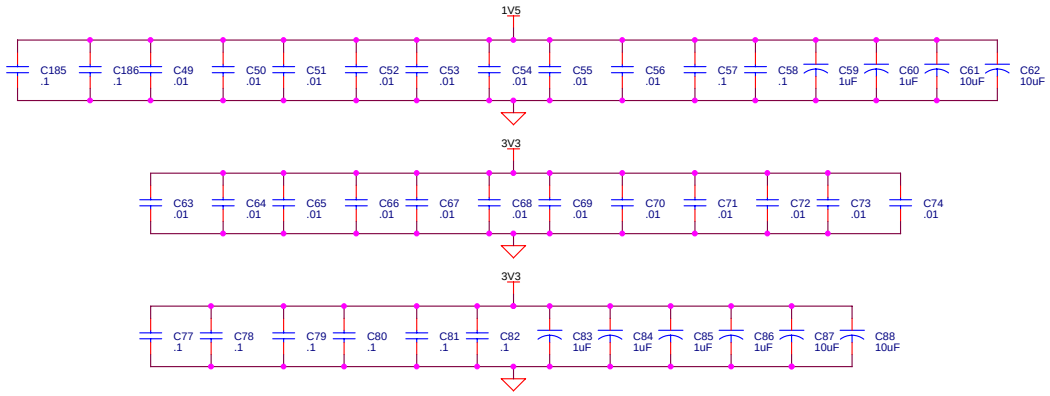
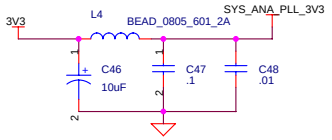
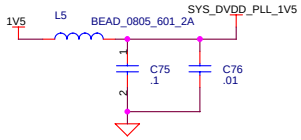


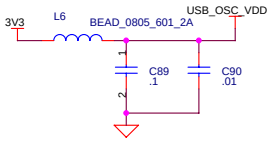


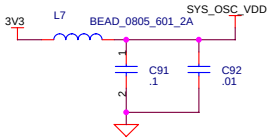
Notice

Isolated power planes are recommended for the NS9360 's 3V3 and 1V5 power pins. See NS9360 design rules found on http://www.digi.com (Support, Documentation)









Title	NS9360 Power Supply pins and filter caps	
	NS9360 Development Board	
Size B	Document Number 30006401-02	Rev D
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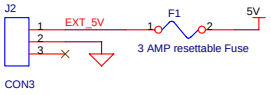
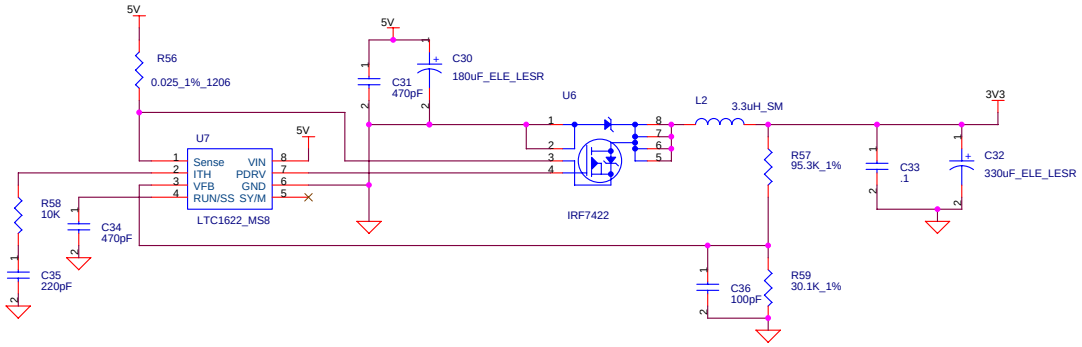
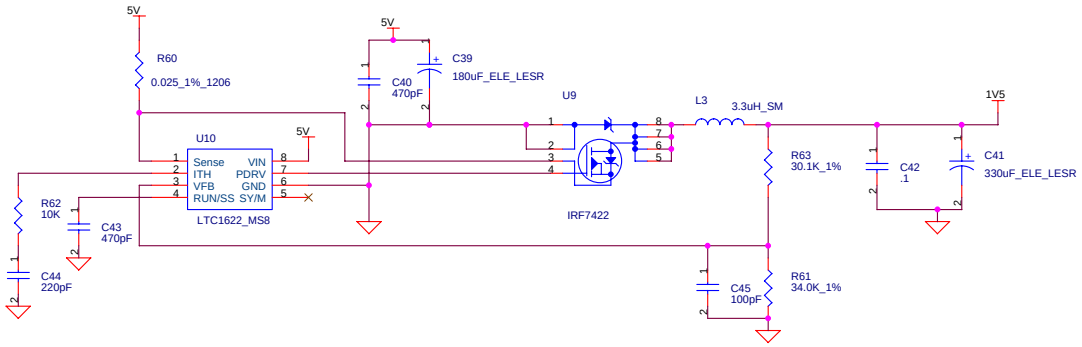


Center Pin +, 5.5mm





Important Disclaimer:

"This power supply design may not meet the latest, required power supply sequencing. See the NS9360 Hardware Reference Guide or Data Sheet for power sequencing specification, or consult factory for power supply design examples".

Power Supply		
Title: NS9360 Development Board		
Size: B	Document Number: 30006401-02	Rev: D
Date: Thursday, May 04, 2006	Sheet 12 of 12	