NS9360 Design Rules
30-Jun-05

A. NS9360 Memory bus termination basic rules.

At 88MHz bus speed and 5 inch traces, the Memory bus can drive four loads without use of buffers.

No Local trace length should exceed 5 inches (127mm). With shorter traces and slower bus speeds more loads may be possible.

Each inch of trace adds 180pS based on 3.3pF per/inch.

SDRAM termination:
All lines to the SDRAM should be terminated.
Address and control terminators are placed as close as possible to NS9360. Data originates at both ends of the bus, so two sets of terminators should be used if traces are 4 inches or greater. One set close to the NS9360, and one close to the SDRAM. If traces are short, place data bus termination close to the NS9360 only. Simulations suggest values of 22 ohms for the series terminations on the address and control lines, and 10 ohms for the terminations on the data lines.

If there are more than four loads, buffer(s) are required, with the buffer being the forth load.
Address lines that connect to Flash or Output buffer(s) only do not need to have series termination.
Data line terminators placed close to Flash are not required. All can share the same data line terminators placed close to the NS9360. Flash is Async, slow speed, and low drive.

SDRAM must remain local.
If the buffer has high drive and traces 4 inches or greater, data line terminators are recommended placed close to the buffers.

Clock Feedback trace length should be 2 to 3 inches (50 to 75mm)
This length strikes a balance between two data paths. One data path is from the SDRAM into the chip (Path A) and the other is from the feedback clock domain back into the AHB clock domain (Path B). Making the feedback clock trace longer helps Path A and hurts Path B. Making the feedback clock trace shorter has the opposite effect. Quite a bit of number crunching shows that a 2 to 3 inch feedback clock trace strikes an optimal balance.
See B. NS9360 SDRAM clock termination.

Most nets on the memory bus will require termination, or at least the provision for termination. The lack of transmission line simulation (Spice or SpectraQuest) for critical nets means some tinkering may still be required during lab test.

A PCB with a Minimum of six layers is recommended.
layer 1 Component Side
layer 2 GND Plane
layer 3 Signal 1
layer 4 Signal 2
layer 5 VCC Plane
layer 6 Solder Side

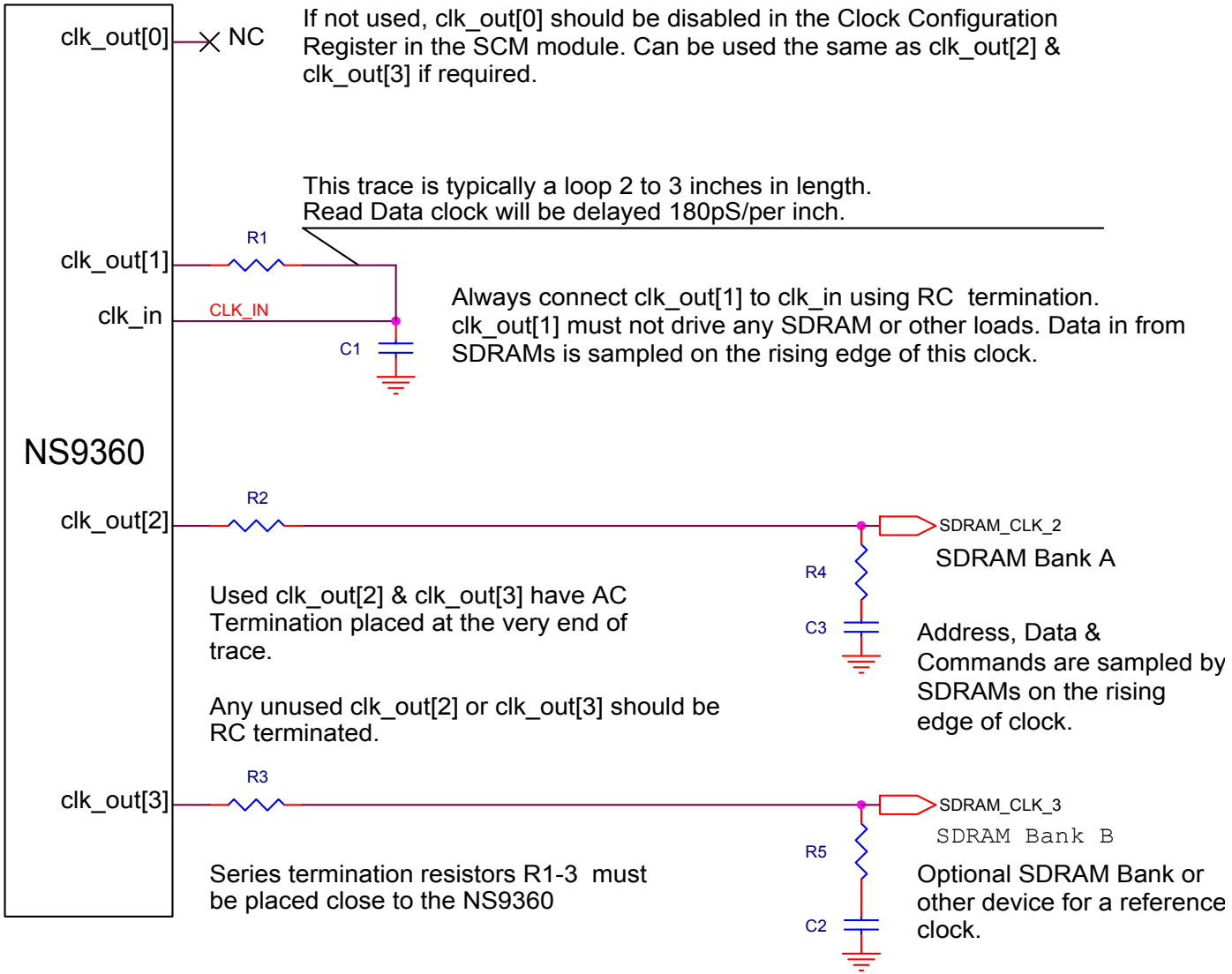
High speed SDRAM clocks and control lines should be buried in the inner layers for lower EMI generation.
Clock lines require separation form other signals - This can be obtained by providing double spacing.

The 3.3V and 1.5V power supplies must have less than 100mV of noise.

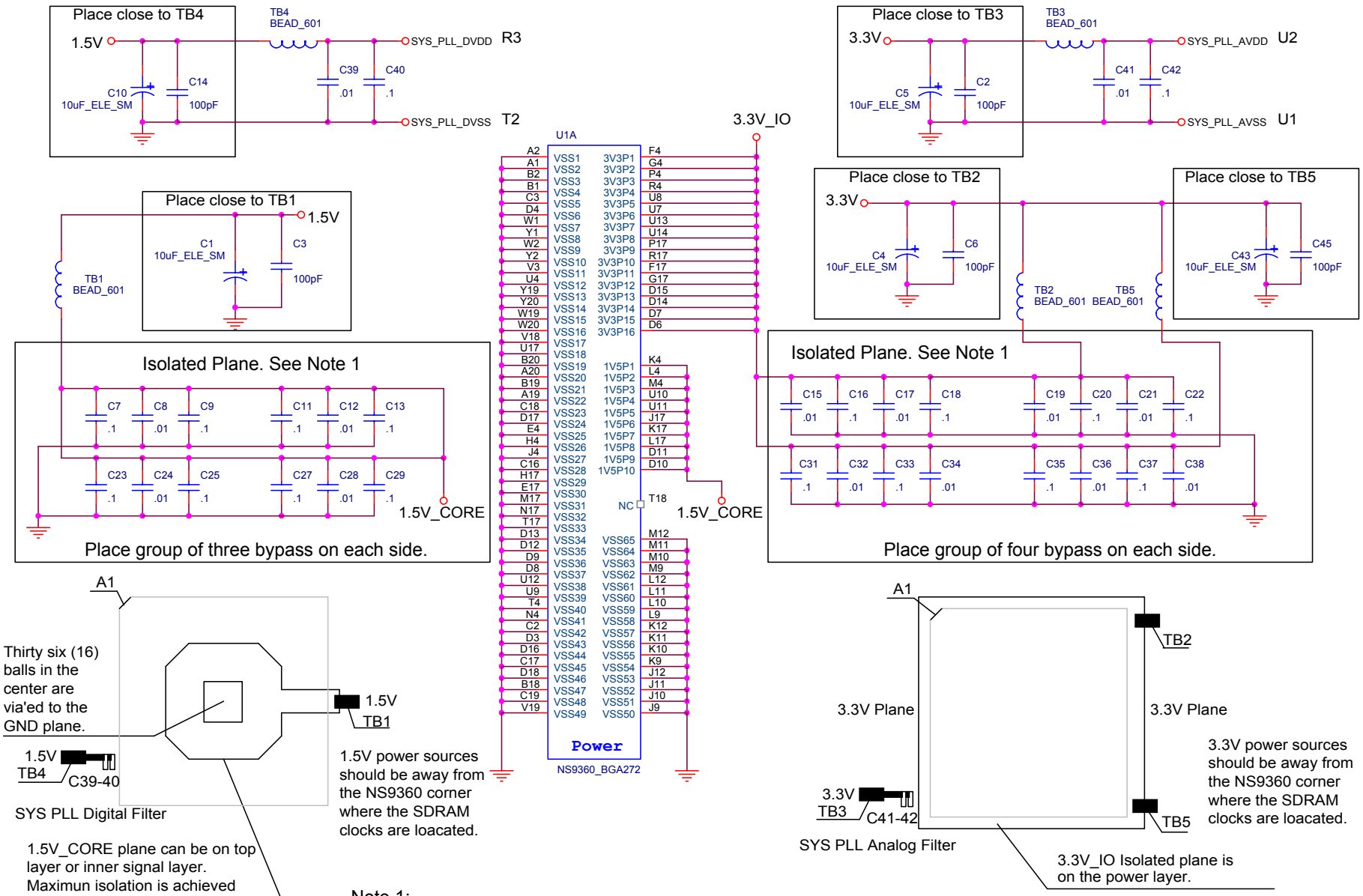
Power sequencing is required. See drawing HRG for an example.

SDRAM must have a generous supply of 100nf and 10nf bypass capacitors.

B. NS9360 SDRAM clock termination



C. NS9360 bypass and power plane recommendations.



Note 1:

These are 3.3V_IO & 1.5V_CORE isolated power planes under the NS9360. Place bypass on the bottom side around the inner row of BGA balls; Connect directly to 1V5 & 3V3 power ball vias when possible. There must be at least one solid GND plane under the NS9360 that is not isolated.