



Note-1 Port Size determines which Byte Enable signals are active.  
8-bit port = BE3\*, 16-bit port = BE[3:2], 32-bit port = BE[3:0]  
Note-2 The Precharge and/or the Active commands are not always present. They depend on the address of the previous SDRAM access.  
Note-3 If CAS Latency = 3 then there are 5 NOPs between the Read and Burst Terminate commands  
Note-4 If CAS Latency = 3 then there are 3 Inhibits after Burst Terminate.  
Note-5 The TA\*/LAST signals are for reference only.

SD\_bst\_Rd.td SDRAM Burst Read, Cas Latency = 2 t16-1