NET+50 to NS9215 Migration Guidance

Revision A1

August 2008

Table of Contents

Overview 4
Software Porting 5
Hardware Design 6
- NET+50 vs. NS921x 6
- Package 7
- Vcore Voltage 7
- Clock Source 7
- Crystal Circuit 8
- Write Enable 8
- CS0WE# and CS0OE# 8
- SDRAM 8
- PHYs w/MII Signal Bootstrapping 8
- Address Line BootStrap 9
- Ports A, B, and C 9
- Ports D, E, F, G, and H 9
- External Chip Select Termination 10
- Bootstrap Pull-Down Resistors 10
- JTAG Debugger 10
  - Hard Reset 10
  - Download Speed 10
- New Features (NS921x) 10
- General 10
- FIMs 11

Commented Schematics 12
Change Log 12

Overview

This document provides general guidance for customers interested in migrating existing product designs based on the obsolete NET+50 processor to the new Digi NS921x processor family by outlining the design modification related aspects that need specific attention.

This document focuses on the Dig NS9215 processor due to its more universal fit for existing NET+50 customers related to the number of available GPIO options. However, the general hardware design aspects described in this document also apply to the NS9210. Designs requiring fewer GPIOs may be able to utilize the Digi NS9210 processor. For example, using Ethernet, 32-bit data bus, and ADDR[27:24] the NS9210 offers 16 available GPIOs.

The Digi NS9215 offers speed grades up to 150 MHz, integrated cache, a NIST-compliant 256-bit AES accelerator, Digi's patented dynamic power management, and features such as up to 4 high-speed UARTs, SPI with boot functionality, fast-mode I2C, ADC, quadrature decoder, PWM, POR, RTC, ten general purpose timers/counters, access to up to 2 Flexible Interface Modules, and 108 multiplexed GPIOs.

The Digi NS9210/NS9215 product brief on the Digi website provides an overview of the key features.

Please refer to the current revision of the Digi NS9210/9215 Hardware Reference Manuals for detailed technical information about the processors and their design characteristics.

A number of Digi partners are also offering NET+50 design migration assessment services. Please contact your local Digi sales representative to discuss available options in your particular region.

Software Porting

The Digi NS921x processor platform is supported in NET+OS® version 7.4 (and greater). NET+OS 7 provides a breadth of new features including an IPv4/v6 dual-mode stack, and the professional Eclipse® based integrated development environment Digi ESP™ with integrated support for the Digi JTAG Link USB 2.0 debugger.

The NET+OS 7 development kits for the NS9210 (Digi P/N NS-9210-NET) and NS9215 (Digi P/N NS-9215-NET) processors include:

- Quick start guide
- Development board
- NS921x processor module
    - 150 MHz, 4 MB Flash, 8 MB SDRAM
- Digi JTAG Link USB 2.0 debugger
    - Digi ESP and CLI support
- Digi NET+OS 7 CD
    - NET+OS 7.x, Digi ESP IDE
- BSP source code, sample code
- Documentation, schematics, and BOMs
- Power supply and accessories
- 1-Year Premium Support contract
    - NS921x hardware with NET+OS 7 software platform
- Free Digi design review
    - NS921x based hardware

In order to migrate a NET+50 design to the NS921x processors, customers need to port their existing NET+OS applications to the NET+OS 7 platform. The NET+50 processor platform is also fully supported in NET+OS 7, which provides customers with the option of first moving their software application from a previous NET+OS version to NET+OS 7 to verify the functionality of the ported software application on their existing NET+50 hardware design. After successful verification in the NET+OS 7 environment, the ported application can be directly moved to the new NS921x based hardware design (BSP).

For customers already using the NET+OS 6.x platform, general NET+OS application software migration information (not hardware platform specific) is also available.

The standard embedded development environment for NET+OS 7 is Digi ESP. However, the third party MULTI IDE from Green Hills Software is still supported by NET+OS 7. If you are planning on using MULTI on the NS921x processor family, please contact your local Digi office to discuss development hardware support and license related aspects.

Hardware Design

NET+50 vs. NS921x

The table below outlines the key differences of the NET+50 and NS921x processors.

Feature/Interface	NET+50	NS9215	NS9210
Core Processor	ARM7TDMI	ARM926EJ-S	ARM926EJ-S
Processor/Bus Speed	44/44 MHz	150/75 MHz max	150/75 MHz max
Cache	8k mixed D/I Cache (Von Neumann)	4k D-Cache 4k I-Cache (Harvard)	4k D-Cache 4k I-Cache (Harvard)
Package	208-pin BGA 15x15 mm, [PQFP]	265-pin BGA 15x15 mm	177-pin BGA 13x13 mm
Cache/RAM Block Options	2k cache / 4k RAM (total of 4 sets)	-	-
Ethernet MAC	10/100 2KB Rx/128-Byte Tx	10/100 2KB Rx/256-Byte Tx	10/100 2KB Rx/256-Byte Tx
AES Accelerator	-	Yes	Yes
UART	2 (230 Kbps)	4 (1.843 Mbps max)	4[2] (1.843 Mbps max)
SPI	2	1 (33 Mps/7.5 Mpbs max) w/boot	1 (33 Mps/7.5 Mpbs max) w/boot
I2C	-	1	1
FIM	-	2	2[3]
ADC	-	1	-
GPIO	24 I/O 16 I/O[1] 16 Input-Only[1]	108 (5V-tolerant Inputs)	54 (5V-tolerant Inputs)
ENI[1]	64k Shared RAM (Slave)	-	-
IEEE1284[1]	4 (Host)	-	-
Timers	2 (27-bit)	10 (32-bit)	10 (32-bit)
PWM	-	4	4
Quadrature Decoder	-	Yes	Yes
POR	-	Yes	-
RTC	-	Battery-backed, With 64 Byte NVRAM	-
Power Management	-	Automatic Clock Scaling, Sleep Modes, Disabling of unused system modules	Automatic Clock Scaling, Sleep Modes, Disabling of unused system modules

[1] Provided by NET+50 MIC. Only one of the selected MIC interfaces (1284, ENI, or GPIO) can be operational at any given time.
[2] UART (2 vs.4) availability depending on 16-/32-bit memory bus use.
[3] FIM 0/1 availability depending on 16-/32-bit memory bus use.

Package

Both the NET+50 and the NS9215 are 15 x 15 mm BGA packages. The NS9215 provides a total of 265 pins, and NET+50 provides a total 208 pins. The NS9215 provides additional power pins. Other NS9215 pins are supporting the RTC with battery backup, ADC, and POR (Internal Power on Reset).

The junction temperature of the NS9215 is specified at 125°C max. This temperature is not reached running at full speed in an ambient operating temperature environment of 85°C.

Vcore Voltage

The NET+50 requires 2.5V at 114 mA max.

The NS9215 requires 1.8V at higher current as shown below. The NS9215 also support power management modes and patented dynamic clock scaling for much more power-efficient product designs.

Full Speed with both FIM clocks running		
CPU at 150 MHz running external SDRAM memory test		
External memory / AHB Bus at 75 MHz		
Both PIC clocks running at 300 MHz	3.3V – 42 mA	0.139 W
Ethernet transmitting and receiving packets	1.8V – 489 mA	0.880 W
Total		**1.019 W**

Slower Speed without FIM clocks running		
CPU at 56 MHz running external SDRAM memory test		
External memory / AHB Bus at 56 MHz		
No PIC clocks		
2 UARTs running	3.3V – 29 mA	0.096 W
Ethernet transmitting and receiving packets	1.8V – 224 mA	0.403 W
Total		**0.499 W**

Clock Source

The NET+50 uses 18.432MHz with external PLL filter components

The NS9215 uses 29.4912MHz without any external PLL filter components.

Use of a spread spectrum clock may be required to to reduce EMI with FIMs enabled.

Crystal Circuit
The NS9215 crystal requires a 330R in series with pin L17 (XTAL2). Without this resistor the crystal is being overdriven and could have a shortened life. Crystal overdrive current also causes excessive EMI.

The NET+50 did not require any series resistor.

Write Enable
The NET+50 has two WE# pins. One for dynamic, and one for static memory.

The NS9215 uses pin C7 (DY_ST_WE#) for all memory types.

CS0WE# and CS0OE#
On the NS9215, ADDR[26] and ADDR[27] cannot be used as CS0WE# and CS0OE# to enable boot flash because they initialize in GPIO mode.

SDRAM
On the NS9215, when using 64Mb (2Mx32) SDRAM, ADDR[22] and ADDR[23] connect to the bank selects. The NET+50 uses ADDR[21] and ADDR[22] instead.

The NET+50 requires external glue logic to correct a "Burst Terminate" bus lockup condition. The NS9215 requires no external glue logic. Connecting CKE0, pin B8 to the SDRAM's CKE input enables the power saving "self refresh" mode on the NS9215.

PHYs w/MII Signal Bootstrapping
On the NS9215, the MII port boots up in GPIO mode with internal pull-ups active, which conflicts with Ethernet PHYs using MII signals for bootstrap.

To use this specific type of PHY with the NS9215, the PHY needs to be held in RESET until the code sets this port to MII mode with pull-ups disabled. A GPIO with a 2.4K pull-down can be used to control the PHY Reset input.

Address Line BootStrap

Address Line	NET+50 Function	NS9215 Function
ADDR[27]	Endian configuration; 1 = Big	Endian configuration; 1 = Big
ADDR[26]	Must be set to 1.	Boot mode; 0 - SPI (Port C)
ADDR[25]	Must be set to 1	Reserved
ADDR[24:23]	CS0 bootstrap	ST_CS1 boot strap
ADDR[22:20]	ENI/MIC MODE[2:0]	Reserved
ADDR[19:09]	GEN_ID setting	GEN_ID setting
ADDR[08]	Reserved	Reserved
ADDR[07]	ENI control PSIO	PLL Bypass; 0 = bypass
ADDR0[6]	ENI Control WR_OC	PLL OD[1]
ADDR[05]	ENI Control DINT2	PLL OD[0]
ADDR[04]	ENI Control I_OC	PLL NR[4]
ADDR[03	ENI Control DMAE	PLL NR[3]
ADDR[02]	Reserved	PLL NR[2]
ADDR[01]	ENI Control EPACK	PLL NR[1]
ADDR[00]	ENI Control PULINT	PLL NR[0]

With no pull-downs on ADDR[07:00] and source clock of 29.4912 MHz, the NS9215 boots at 56 MHz CPU/AHB bus speed.

For 44 MHz operation, add 2.4K pull-down resistors on ADDR[03], ADDR[02], and ADDR[01].

Ports A, B, and C

The NET+50 provides two serial ports: A and B. RI# for both ports is on port C.

The NS9215 offers three full serial ports on A, B, and C. Port D can also be utilized as a full serial port, if not used as an ENI/MIC GPIO port.

The NET+50 has 4 mA drive on PORT[C4:0]. The NS9215 provides 2 mA drive on the corresponding pins, GPIO[11:8].

Ports D, E, F, G, and H

This is the NET+50 ENI/MIC port with three modes, preset by ADDR[22:20].

IEEE1284 and FIFO/Shared memory modes are not supported on the NS9215.

ADDR[22:20] are not used for bootstrap.

In GPIO mode, port E is not available on the NET+50. The NS9215 supports all five ports in GPIO mode with 32 external interrupts. When set for external interrupt, the FIMs are used instead.

External Chip Select Termination

Pin A9 (NS_TA_STB) on the NS9215 is similar to TA# on the NET+50. This is an input signal that can be used to add extended wait states for static memory, which can externally terminate the chip select.

Bootstrap Pull-Down Resistors

The NET+50 requires 1.0K pull-down resistors (internal resistor equivalent to 7.8K).

The NS9215 requires 2.4K pull-down resistors (internal resistor equivalent to 16.5K).

JTAG Debugger

Hard Reset

The NET+50 maintains the debugger connection when RESET# (hard reset) is active.

The NS9215 does not maintain the debugger connection when RESET# is active. In order to allow maintaining the debugger connection, the new signal SRESET# has been added on pin D9. For full debugger support pin D9 needs to be connected to the debugger's SRST# pin with a 2.4K pull-up.

Download Speed

The NS9215 can download code from the debugger at faster speeds if the adaptive clocking signal RTCK is brought out to the debugger RTCK input. This new signal is on pin P16. On a 20-pin JTAG connector, the corresponding signal is located on pin 11.

The debugger's speed can be slowed down to work without RTCK. The Debugger's adaptive clocking must be disabled and the RTCK pin input to the debugger should be connected to GND.

New Features (NS921x)

General

A. The GPIO and memory bus inputs are 5V tolerant

B. If the memory bus is x16, then Data[15:0] can be used as GPIO.

C. If the MII bus is not used, these eighteen pins can be used as GPIO.

D. Address lines ADDR[27:24] can be used as GPIO.

E. Address line ADDR[26] pulled down enables SPI boot to SDRAM from GPIO[11] and GPIO[13:15].

F. ADDR[27], pin P12, can be used to supply an external UART reference clock.

FIMs

The unique Flexible Interface Modules (FIMs) on the NS921x processors provide two independent on-chip DRPIC1655X processor cores (up to 300 MHz each) allowing the selection of a growing list of application-specific peripheral interface implementations offered by Digi.

From a software point of view, NET+OS 7 applications utilize the additional FIM-provided interfaces by simply opening the corresponding interfaces through standard NET+OS API calls. The actual initial programming of the FIM is completely abstracted, and the functionality of each interface is seamlessly integrated into the NET+OS framework.

The table below outlines the currently available and planned FIM interfaces (as of August 2008).

Interface	NET+OS 7.4 (and greater) Planned Availability
SD/SDIO	Available
CAN 2.0	Available
USB Device (low-speed)	October 2008
Wiegand	March 2009
I^2S	February 2009
Parallel Bus (Mot/Int)	December 2008
1-Wire	Available
UART w/9 bit support (460k)	Available

Please contact your local Digi sales office to discuss the available options with respect to application/customer specific FIM interface implementations.

Commented Schematics

Commented migration schematics are attached to this PDF document.

If your version of the Adobe® Reader® does not support PDF file attachments, a standalone PDF file of the commented migration guidance schematics is also available on the Digi support website.

Change Log

Revision	Date	Comment
A1	August 2008	New document