High Resolution Pulse Generation

An Application Note for the
NS9360 Processor

Purpose of this document

This application note describes a method for using the NS9360's PWMs to generate high resolution pulses.

It requires one external connection from the PWM output to the pulse timer input and the ability to change registers on command.

Example: Using PWM1

Generating a 20 kHz frequency, 20 μs pulse width:

- Add wire to connect PWM1 output (GPIO37) to Timer2 input (GPIO15)
- Configure GPIO15 as Timer2 input
  - `gpio cfg reg2 addr 9060_0014 bits 31:28 = 'h1`
- Configure GPIO37 as PWM1
  - `gpio cfg reg5 addr 9060_0020 bits 23:20 = 'h8`

Timer2 sets the pulse width, and Timer3 sets the period; Timer2 and Timer3 are configured when the control registers are set (see below).

Reload Counters (assume CPUclock/4 is set in the Timer Control Register)

- Timer2 — `A090_004C 0000_0375`
  - pulse width = 4(CPUclk_period)(pulse width count)
- Timer3 — `A090_0050 0000_08A4`
  - period = 4(CPUclk_period)(period count)

20 kHz gives us a 50 μs period

177 MHz (176.9472) gives us a 5.6514 ns CPUclk_period

period count = 50 μs / (4 * 5.6514 ns) = 2211.84
rounded to 2212, or 0x8A4

pulse width = 20 μs

pulse width count = 20 μs / (4 * 5.6514 ns) = 884.73
rounded to 885, or 0x375

Control Registers

- Timer2 `A090_0198 0000_80A7`
  - Timer enabled, CPUclock/4, external high-gated, counts down, 32-bit, reload enabled
- Timer3 `A090_019C 0000_8087`
  - Timer enabled, CPUclock/4, internal, counts down, 32-bit, reload enabled

In this specific example using a 177 MHz CPU clock and timers set to CPUclock/4 mode, the resolution is 22.6 ns; otherwise stated as (1/2212) or 0.045%.

PWM Output: Special Cases

There is approximately one (1) period delay from the start of the period timer to the generation of the first pulse. There is a delay of up to two (2) periods from the point when the new pulse count is written in the reload register to the point when the new pulse width takes effect, depending on the current duty cycle and when the write occurs relative to the end of a pulse.

When pulse count = period count

PWM output is always high

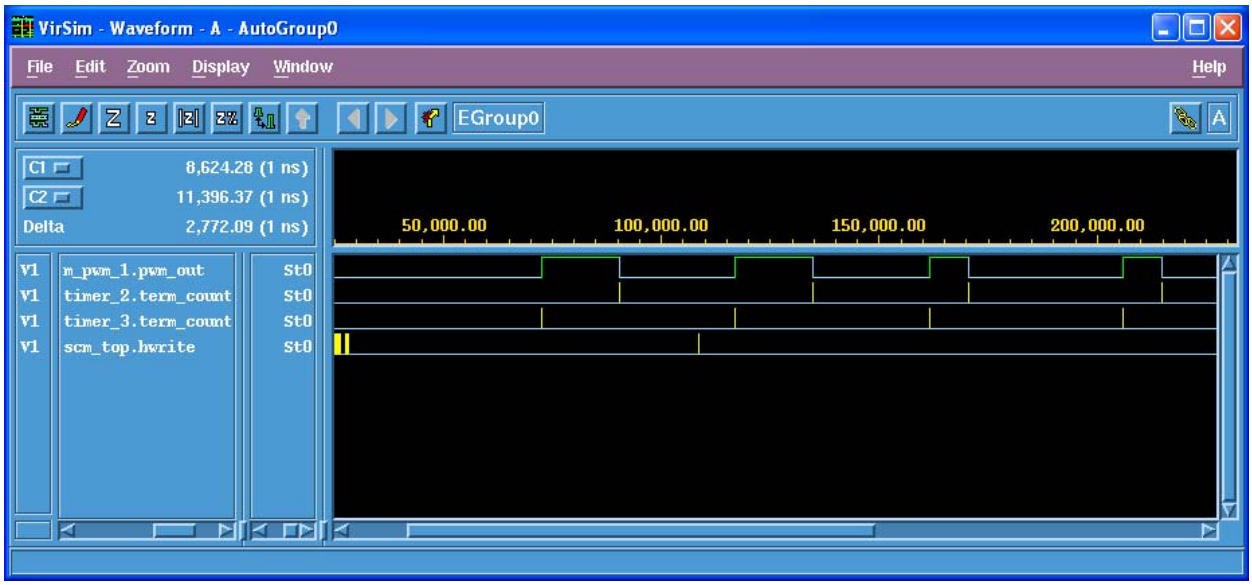
When pulse count = 0

PWM output is a one (1) CPUclock-wide pulse

The following steps may be used to halt the PWM output in the low state:

- Write to the reload count register of the timer controlling the period with the maximum count. As this is a 32-bit counter, this number is 0xFFFF_FFFF.
- Wait one full “old” period time to ensure the new count value has been loaded.
- Disable both timers.

Example: Graphical Representation



Example starting with a 40% duty cycle for the first two pulses, then changing to 20%:

The **scm_top.hwrite** signal at approximately 108,000.00 shows where the pulse reload count register is updated. The new count value is loaded into the counter at the end of the next 40% duty cycle pulse and is used to generate the 20% duty cycle pulse that follows.

Conditions and Further Information

TLCS set to 000 or 001 in timer control register

Note: With very short period or pulse counts (<4), the PWM does not function correctly. With period or pulse counts greater than or equal to 4, the period or pulse will be one (1) CPU clock cycle longer than programmed.

For further information on the operation of the NS9360 processor, please consult the support documentation, available online at:

http://www.digi.com/products/embeddedsolutions/ns9360.jsp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