RABBIT® 6000 MICROPROCESSOR

REFERENCE

REGISTER LEGEND

Read/Write | Write Only | Read Only

Read (Special Behavior on Write Operation)

NOTE: ZERO MUST BE WRITTEN TO ALL UNUSED BITS

Processor Control

GLOBAL CLOCK MODULATOR REGISTERS
GCM0R (0x00A)

00 = 1 ns DITHER
01 = 0.5 ns DITHER
10 = 2 ns DITHER
RESERVED MUST = 0
SYSTEM PLL LOOP DIVIDER

GCM1R (0x00BB)

0 = SPREADER OFF
1 = SPREADER ON
RESERVED MUST = 0
SYSTEM PLL PREDIVIDER

GLOBAL POWER SAVE CONTROL REGISTER
GPSCR (0x0000)

000 = SELF-TIMED CS DISABLE
001 = 230 ns
010 = 170 ns
011 = 110 ns
100 = 290 ns
101 = 230 ns
110 = 170 ns
111 = 110 ns
SELF-TIMED CS READ AND WRITE
SELF-TIMED CS READ ONLY
0 = NORMAL CS FOR READS
1 = SHORT CS TIMING FOR READS*
0 = NORMAL CS FOR WRITES
1 = SHORT CS TIMING FOR WRITES*
000 = 32 kHz
001 = RESERVED
100 = 16.3848 kHz
101 = 8.192 kHz
110 = 4.096 kHz
111 = 2.048 kHz
CPU & PCLK

#NOT AVAILABLE AT FULL SPEED!

GLOBAL CLOCK CONFIGURATION REGISTER
GCFG (0x002F)

GLOBAL REVISION REGISTER
GREV (0x002F)

0 = FETCH PER SMODE
1 = IGNORE SMODE
RD ONLY
SMODE
CPU VERSION (GCPU)
REVISION (GREV)

MASTER SYSTEM STATUS REGISTER
MSSR (0x0435)

0 = WIFI DIRECT CLOCK
1 = WIFI EXTERNAL XTAL
0 = USB DIRECT CLOCK
1 = USB EXTERNAL XTAL
0 = RC WIFI PLL NOT READY
1 = RC WIFI PLL READY
0 = RC SYSTEM PLL NOT READY
1 = RC SYSTEM PLL READY

GLOBAL CONTROL/STATUS REGISTER
GCSR (0x000D)

000 = NO TIMEOUT
010 = WATCHDOG TIMEOUT
110 = HARDWARE RESET
111 = POWER-ON RESET
STATUS OUTPUT
00 = LOW DURING FIRST OPCODE FETCH
01 = LOW DURING INTERRUPT ACKNOWLEDGE
10 = LOW
11 = HIGH
/WDTOUT OUTPUT
00 = LOW DURING WDT TIMEOUT
01 = TEST MODE (INTERNAL USE)
10 = LOW PULSE (1–2 CYCLES @ 32 kHz)
11 = HIGH
/BUFEN OUTPUT
00 = LOW FOR EXTERNAL I/O CYCLE
01 = LOW FOR DATA MEMORY ACCESS
10 = LOW
11 = HIGH
OSC
000 = CPU = OSC/8, PCLK = OSC/8
001 = CPU = OSC/8, PCLK = OSC
010 = CPU = OSC, PCLK = OSC
011 = CPU = OSC/2, PCLK = OSC/2
100 = CPU = OSC/4, PCLK = OSC/4
MAIN OSC ON
MAIN OSC OFF
101 = CPU = 32 kHz, PCLK = 32 kHz; MAIN OSC ON
110 = CPU = OSC/4, PCLK = OSC/4
PERIODIC INTERRUPT
00 PERIODIC INTERRUPT = DISABLE
01 PERIODIC INTERRUPT = PRIORITY 1
10 PERIODIC INTERRUPT = PRIORITY 2
11 PERIODIC INTERRUPT = PRIORITY 3
PERIODIC INTERRUPT = 32 kHz/16 (488 ms)
CPU = CPU CLOCK
CPU = CPU CLOCK
OSC = DOUBLED OR NON-DOUBLED CLOCK

GLOBAL CLOCK DOUBLE REGISTER
GCDR (0x000F)

0 = DISABLE SYSTEM PLL
1 = ENABLE SYSTEM PLL
RESERVED MUST = 0
CLOCK DOUBLE DISABLED
CLOCK DOUBLE ENABLED, TYPICAL CLOCK LOW TIME

PROCESSOR MODE SELECT

SMODE1	SMODE0	BOOTSTRAP OPERATION
0	0	BOOTSTRAP DISABLED, NORMAL PROCESSOR OPERATION/CODE FETCHED FROM MEMORY)
0	1	SLAVE PORT. SPDDR USED FOR BOOTSTRAP OPERATION
1	0	SYNCHRONOUS SERIAL. CLOCKED SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. MAX EXTERNAL CLOCK RATE = PCLK/6
1	1	ASYNCHRONOUS SERIAL. ASYNCH SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. REQUIRED BAUD RATE = 2400

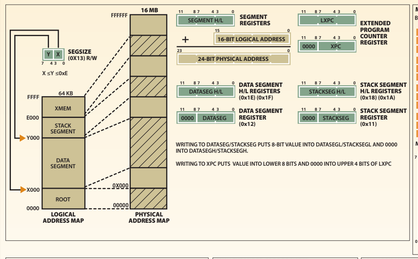
PIN CONTROL REGISTERS
ADPCR (0x40A0)
CPCR (0x04A3)
IOPCR (0x04A3)

0 = FAST OUTPUT SLEW
1 = SLOW OUTPUT SLEW
00 = 4mA OUTPUT DRIVE
01 = 8mA OUTPUT DRIVE
10 = 10mA OUTPUT DRIVE
11 = 14mA OUTPUT DRIVE
00 = NO PULLUP/DOWN
01 = 750KOHM PULLUP
10 = 750KOHM PULLDOWN
11 = 750KOHM KEEPER

DATA BUS PIN CONTROL REGISTER
DOPCR (0x04A1)

0 = FAST OUTPUT SLEW
1 = SLOW OUTPUT SLEW
00 = 4mA OUTPUT DRIVE
01 = 8mA OUTPUT DRIVE
10 = 10mA OUTPUT DRIVE
11 = 14mA OUTPUT DRIVE
00 = NO PULLUP/DOWN
01 = 750KOHM PULLUP
10 = 750KOHM PULLDOWN
11 = 750KOHM KEEPER

Memory Management Unit



SEGMENT REGISTERS

15	8	7	4	3	0
SEGMENT H/L				LXPC	
15	8	7	4	3	0
0000	24-BIT LOGICAL ADDRESS			0000	XPC

DATA SEGMENT H/L REGISTERS (0x18) (0x1)

DATA SEGMENT REGISTER (0x12)

EXTENDED PROGRAM COUNTER REGISTER

STACK SEGMENT H/L REGISTERS (0x1B) (0x1A)

STACK SEGMENT REGISTER (0x11)

WRITING TO DATASEG/STACKSEG PUTS 8-BIT VALUE INTO DATASEG/STACKSEG, AND 0000 INTO DATASEG%/STACKSEG%.

WRITING TO XPC PUTS VALUE INTO LOWER 8 BITS AND 0000 INTO UPPER 4 BITS OF LXPC

MEMORY BANK CONTROL REGISTERS

BANK SELECT BITS	CONTROL REGISTER USED	ADDRESS
00x	MB0CR	(0x0014)
000	MB0CR	(0x0400)
001	MB0HCR	(0x0401)
01x	MB1CR	(0x0015)
010	MB1CR	(0x0402)
011	MB1HCR	(0x0403)
10x	MB2CR	(0x0016)
100	MB2CR	(0x0404)
101	MB2HCR	(0x0405)
11x	MB3CR	(0x0017)
110	MB3CR	(0x0406)
111	MB3HCR	(0x0407)

MBxCR: 0 = 4 WS (5 FOR WRITES); 1 = 2 WS (3 FOR WRITES); 10 = 1 WS (2 FOR WRITES); 11 = 0 WS (1 FOR WRITES)
0 = PASS BANK SEL ADDR MSB
1 = INVERT BANK SEL ADDR MSB
0 = PASS BANK SEL ADDR LSB
1 = INVERT BANK SEL ADDR LSB
00 = /OE0 AND /WE0 ARE ACTIVE
01 = /OE1 AND /WE1 ARE ACTIVE
10 = /OE0 IS ACTIVE (READ ONLY)
11 = /OE1 IS ACTIVE (READ ONLY)
00 = /CS0 IS ACTIVE
01 = /CS1 IS ACTIVE
10 = /CS2 IS ACTIVE
11 = /CS3 (INTERNAL MEM) IS ACTIVE

ADVANCED CHIP SELECT CONTROL REGISTERS
ACSCR (0x0410) ACS1CR (0x0411)
ACS2CR (0x0412)

000 = 0 EXTRA WS (RD, WR, 1st PAGE READ)
001 = 1 EXTRA WS (RD, WR, 1st PAGE READ)
010 = 2 EXTRA WS (RD, WR, 1st PAGE READ)
011 = 3 EXTRA WS (RD, WR, 1st PAGE READ)
100 = 4 EXTRA WS (RD, WR, 1st PAGE READ)
101 = 5 EXTRA WS (RD, WR, 1st PAGE READ)
110 = 6 EXTRA WS (RD, WR, 1st PAGE READ)
111 = 7 EXTRA WS (RD, WR, 1st PAGE READ)
000 = 0 EXTRA WS (LATER PAGE READS)
001 = 1 EXTRA WS (LATER PAGE READS)
010 = 2 EXTRA WS (LATER PAGE READS)
011 = 3 EXTRA WS (LATER PAGE READS)
0 = NO ADDITIONAL WAIT STATES
1 = ADD 8 WAIT STATES
0 = PAGE SIZE 16 BYTES
1 = PAGE SIZE 8 BYTES
0 = DISABLE BYTE WRITES ON 16-BIT BUS
1 = ENABLE BYTE WRITES ON 16-BIT BUS

RAM SEGMENT REGISTER
RAMSR (0x0448)

COMPARE VALUE FOR RAM SEGMENT LIMIT CHECKING

0 = DISABLE RAM SEGMENT LIMIT CHECKING
1 = SELECT DATA MMU TRANSLATION IF PC[15:12] = RAMSR[7:4]
0 = SELECT DATA MMU TRANSLATION IF PC[15:12] = RAMSR[7:4]

MEMORY TIMING CONTROL REGISTER
MTCR (0x0019)

0 = NO INTERNAL WRITE WAIT STATES
1 = ADD INTERNAL WRITE WAIT STATE
0 = NORMAL TIMING
1 = EXTENDED TIMING

MMU INSTRUCTION/DATA REGISTER
MMIDR (0x0010) R/W

0 = USE 8-BIT INTERNAL I/O ADDRESSES
1 = USE 16-BIT INTERNAL I/O ADDRESSES
RESERVED WRITE MUST = 0
0 = ALL MSB INVERSION INDEPENDENT OF INSTRUCTION/DATA
1 = A16, MSB INVERSION FOR DATA ACCESS ONLY.
(THIS ENABLES SEPARATE I AND D SPACE)
0 = NORMAL /CS1 OPERATION
1 = FORCE /CS1 ALWAYS ACTIVE
0 = NORMAL
1 = INVERT MSB ON DATASEG ACCESS
0 = NORMAL
1 = INVERT A16 ON DATASEG ACCESS
0 = NORMAL
1 = INVERT BANK SEL ADDR MSB ON ROOT ACCESS
0 = NORMAL
1 = INVERT A16 ON ROOT ACCESS

MMU EXPANDED CODE REGISTER
MECR (0x0018)

1000 = BANK SELECT ADDRESS IS A [19:18]
001 = BANK SELECT ADDRESS IS A [20:19]
010 = BANK SELECT ADDRESS IS A [21:20]
011 = BANK SELECT ADDRESS IS A [22:21]
100 = BANK SELECT ADDRESS IS A [23:22]
111 = BANK SELECT ADDRESS IS A [18:17]
OTHERS RESERVED
0000 = NORMAL
0100 = USE MB0CR FOR XPC ACCESS
0101 = USE MB1CR FOR XPC ACCESS
0110 = USE MB2CR FOR XPC ACCESS
0111 = USE MB3CR FOR XPC ACCESS
1100 = USE MB0HCR FOR XPC ACCESS
1101 = USE MB1HCR FOR XPC ACCESS
1110 = USE MB2HCR FOR XPC ACCESS
1111 = USE MB3HCR FOR XPC ACCESS

MEMORY ALTERNATE CONTROL REGISTER
MACR (0x0010)

0 = NORMAL 8-BIT OPERATION FOR /CS3
1 = NORMAL 16-BIT OPERATION FOR /CS3
0 = NORMAL 8-BIT OPERATION FOR /CS2
01 = PAGE-MODE 8-BIT OPERATION FOR /CS2
10 = NORMAL 16-BIT OPERATION FOR /CS2
11 = PAGE-MODE 16-BIT OPERATION FOR /CS2
0 = NORMAL 8-BIT OPERATION FOR /CS1
01 = PAGE-MODE 8-BIT OPERATION FOR /CS1
10 = NORMAL 16-BIT OPERATION FOR /CS1
11 = PAGE-MODE 16-BIT OPERATION FOR /CS1
0 = NORMAL 8-BIT OPERATION FOR /CS0
01 = PAGE-MODE 8-BIT OPERATION FOR /CS0
10 = NORMAL 16-BIT OPERATION FOR /CS0
11 = PAGE-MODE 16-BIT OPERATION FOR /CS0

Direct Memory Access

NOT ALL REGISTERS DISPLAYED; SEE PROCESSOR MANUAL FOR MORE DETAILS.

DMA MASTER CONTROL/STATUS REGISTER
DMACSLR (0x0100) DMACSMR (0x0101)

WR 0 = NO EFFECT
WR 1 = START/RESTART CHANNEL
RD 0 = CHANNEL DISABLED
RD 1 = CHANNEL ENABLED

DMA MASTER CONTROL REGISTER
DMCR (0x0104)

00 = DISABLE INTERRUPT
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT
0 = PRIORITY 0 TRANSFER
1 = PRIORITY 1 TRANSFER
10 = PRIORITY 2 TRANSFER
11 = PRIORITY 3 TRANSFER

DMA MASTER TIMING CONTROL REGISTER
DMTCR (0x0105)

0x = FIXED DMA CHANNEL PRIORITY
10 = ROTATE PRIORITY AFTER EVERY BYTE
11 = ROTATE PRIORITY AFTER EVERY REQUEST
000 = MAX 1 BYTE BURST
001 = MAX 2 BYTE BURST
010 = MAX 4 BYTE BURST
011 = MAX 8 BYTE BURST
100 = MAX 16 BYTE BURST
110 = MAX 32 BYTE BURST
111 = MAX 64 BYTE BURST
000 = MIN 13 CLOCKS BETWEEN BURSTS
001 = MIN 14 CLOCKS BETWEEN BURSTS
010 = MIN 24 CLOCKS BETWEEN BURSTS
011 = MIN 48 CLOCKS BETWEEN BURSTS
100 = MIN 96 CLOCKS BETWEEN BURSTS
101 = MIN 128 CLOCKS BETWEEN BURSTS
110 = MIN 256 CLOCKS BETWEEN BURSTS
111 = MIN 512 CLOCKS BETWEEN BURSTS

DMA μ BUFFER COMPLETE REGISTER
DMBCR (0x0107)

WR = LOAD COUNTER
RD = READ COUNTER

DMA μ BUFFER UNUSED (7:0) REGISTER
D0BU0R-D7BU0R (0x01yA)
D0BU0R-D15BU0R (0x09yA)

DMA μ BUFFER UNUSED (15:8) REGISTER
D0BU1R-D7BU1R (0x01yB)
D0BU1R-D15BU1R (0x09yB)

STORES BITS OF BUFFER UNUSED LENGTH VALUE

DMA MASTER AUTO-LOAD REGISTER
DMALLR (0x0110)
DMALMR (0x0111)

0 = NO EFFECT
1 = AUTO-LOAD CHANNEL

DMA TIMED REQUEST DIVIDER HIGH REGISTER
DTDRHR (0x0117)

MSB OF LIMIT VALUE FOR TIMER

DMA TIMED REQUEST DIVIDER LOW REGISTER
DTDRLR (0x0116)

LSB OF LIMIT VALUE FOR TIMER

DMA SPECIAL CONTROL REGISTER
D0SCR (0x0140) ... D15CR (0x0150)
D2SCR (0x0140) ... D3SCR (0x01B0)
D4SCR (0x01C0) ... D5SCR (0x01D0)
D6SCR (0x01E0) ... D7SCR (0x01F0)

0X = NORMAL DMA OPERATION
10 = ENABLE DMA FOR USB RX
11 = ENABLE DMA FOR USB TX
0 = AUTOMATIC SELECTION OF CYCLE-STEAL MODE
1 = DISABLE CYCLE-STEAL MODE
0 = AUTO-CONNECT SOURCE DMA REQUEST
1 = DISCONNECT SOURCE DMA REQUEST
0 = NORMAL SOURCE ADDRESS
1 = FIXED SOURCE ADDRESS
0 = AUTO-CONNECT DEST DMA REQUEST
1 = DISCONNECT DEST DMA REQUEST
0 = NORMAL DEST ADDRESS
1 = FIXED DEST ADDRESS

DMA CYCLE-STEAL TIMING CONTROL REGISTER
DCSTCR (0x0125)

0 = FIXED DMA CHANNEL PRIORITY
10 = ROTATE PRIORITY AFTER EVERY BYTE
11 = ROTATE PRIORITY AFTER EVERY REQUEST
000 = MAX 1 BYTE BURST
001 = MAX 2 BYTE BURST
010 = MAX 4 BYTE BURST
011 = MAX 8 BYTE BURST
100 = MAX 16 BYTE BURST
110 = MAX 32 BYTE BURST
111 = MAX 64 BYTE BURST

DMA DESCRIPTOR REGISTER
ADD MULTIPLE OF 0x10 FOR CHANNELS 1 THRU 7; ADD 0x800 FOR CHANNELS 8 THRU 15

D0CR (0x0181) ... D7CR (0x01B1) — SEE BIT SETTINGS BELOW
D0LR (0x0182) ... D7LR (0x01B2) — DMA LENGTH
D0SAR (0x0184) ... D7SAR (0x01B4) — DMA SOURCE ADDRESS
D0DAR (0x0188) ... D7DAR (0x01B8) — DMA DEST ADDRESS
D0LAR (0x018C) ... D7LAR (0x01BC) — DMA LINK ADDRESS

DMA x CONTROL REGISTER
D0CR (0x0181)

0 = CONTINUE TO NEXT BUFFER DESCRIPTOR
1 = FINAL BUFFER DESCRIPTOR
0 = USE SEQUENTIAL ADDRESS
1 = USE LINK ADDRESS FIELD
0 = NORMAL
1 = SPECIAL LAST BYTE
0 = NO INTERRUPT ON COMPLETION
1 = INTERRUPT ON COMPLETION
00 = SOURCE ADDRESS IS FIXED INTERNAL I/O ADDRESS
01 = SOURCE ADDRESS IS FIXED EXTERNAL I/O ADDRESS
10 = SOURCE ADDRESS IS MEMORY ADDR, AUTO-INCREMENT
11 = SOURCE ADDRESS IS MEMORY ADDR, AUTO-INCREMENT
00 = DESTINATION ADDRESS IS FIXED INTERNAL I/O ADDR
01 = DESTINATION ADDRESS IS FIXED EXTERNAL I/O ADDR
10 = DESTINATION ADDRESS IS MEMORY ADDR, AUTO-INCREMENT
11 = DESTINATION ADDRESS IS MEMORY ADDR, AUTO-INCREMENT

DMA MASTER HALT REGISTER
DMHLR (0x0102)
DMHMR (0x0121)

0 = NO EFFECT
1 = HALT CHANNEL

DMA MASTER REQUEST 0 CONTROL REGISTER
DMRRCR (0x0106)

00 = REQUESTS DISABLED
01 = REQUEST ENABLED FROM PD2
10 = REQUEST ENABLED FROM PE2
11 = REQUEST ENABLED FROM IRQ2
0 = FALLING EDGE TRIGGERED (1 BYTE)
1 = RISING EDGE TRIGGERED (1 BYTE)
0 = ACTIVE LOW
1 = ACTIVE HIGH
0 = REQUEST 0 TO THIS DMA CHANNEL
1 = REQUEST 1 TO THIS DMA CHANNEL

DMA MASTER REQUEST 1 CONTROL REGISTER
DMR1CR (0x0107)

00 = REQUESTS DISABLED
01 = REQUEST ENABLED FROM PD3
10 = REQUEST ENABLED FROM PE3
11 = REQUEST ENABLED FROM IRQ3
0 = FALLING EDGE TRIGGERED (1 BYTE)
1 = RISING EDGE TRIGGERED (1 BYTE)
0 = ACTIVE LOW
1 = ACTIVE HIGH
0 = REQUEST 1 TO THIS DMA CHANNEL
1 = REQUEST 0 TO THIS DMA CHANNEL

DMA TIMED REQUEST CONTROL REGISTER
DTRCR (0x0115)

0 = TIMED REQUEST DISABLED
1 = TIMED REQUEST ENABLED
00 = 1 BYTE PER REQUEST
01 = RESERVED
10 = TRANSFER UNTIL BUFFER
11 = TRANSFER IS COMPLETE
11 = RESERVED
REQUEST TO THIS DMA CHANNEL

DMA μ TERMINATION BYTE REGISTER
D0TBR-D7TBR (0x01yB)
D8TBR-D15TBR (0x09yB)

MATCH VALUE

DMA μ TERMINATION MASK REGISTER
D0TMR-D7TMR (0x01yY)
D8TMR-D15TMR (0x09yY)

TERMINATION BYTE MASK

Timer B

TIMER B CONTROL/STATUS REGISTER
TBCSR (0x0080)

(WRITE)
0 = CORRESPONDING INTERRUPT IS DISABLED
1 = CORRESPONDING INTERRUPT IN ENABLED
(READ)
0 = CORRESPONDING HAS NOT ENCOUNTERED A MATCH
1 = A CORRESPONDING INT. HAS ENCOUNTERED A MATCH (STATUS BITS AND INTERRUPTS ARE CLEARED BY READ OF THIS REGISTER)

TIMER B MATCH 1 REGISTER
(MSB) TBM1R (0x0092)
(LSB) TBL1R (0x0083)

TIMER B MATCH 2 REGISTER
(MSB) TBM2R (0x0084)
(LSB) TBL2R (0x0085)

TIMER B COUNT REGISTER
(MSB) TBCMR (0x008E)
(LSB) TBCLR (0x008F)

TIMER B CONTROL REGISTER
TBCR (0x0081)

0 = NORMAL B2 OPERATION
1 = B2 USES STEP REGS
0 = NORMAL B1 OPERATION
1 = B1 USES STEP REGS
00 = CLOCKED BY PCLK/2
01 = CLOCKED BY TIMER A1
10 = CLOCKED BY PCLK/16
11 = CLOCKED BY A11
00 = INTERRUPTS DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT
0 = TIMER B CLOCK (PCLK/2) IS DISABLED
1 = TIMER B CLOCK (PCLK/2) IS ENABLED

TIMER B STEP LSB x REGISTER
TBSLR (0x008A) TBSL2R (0x008C)

TIMER B STEP MSB x REGISTER
TBSMR (0x008B) TBSM2R (0x008D)

LSB OF STEP SIZE FOR COMPARATOR

MSB OF STEP SIZE FOR COMPARATOR

Network Ports

NOT ALL REGISTERS DISPLAYED; SEE PROCESSOR MANUAL FOR MORE DETAILS.

NETWORK PORT C CPU WAIT REGISTER
NCCWR (0x0431)

ONES COMPLIMENT OF WIFI CPU WAIT STATES (0-31)

NETWORK PORT D WAIT REGISTER
NDWR (0x0433)

ONES COMPLIMENT OF USB WAIT STATES (0-31)

NETWORK PORT C DMA WAIT REGISTER
NCDWR (0x0432)

ONES COMPLIMENT OF WIFI DMA WAIT STATES (0-31)

USB WRAPPER REGISTER
USBWR (0x1060)

0 = DISABLE D+ PULLDOWN
1 = ENABLE D+ PULLDOWN
0 = DISABLE D- PULLDOWN
1 = ENABLE D- PULLDOWN
0 = DISABLE USB OVERCURRENT SIGNAL
1 = ENABLE USB OVERCURRENT SIGNAL ON PE3

ENABLE NETWORK PORT REGISTER
ENPR (0x0430)

0 = DISABLE WIFI
1 = ENABLE WIFI
0 = DISABLE ETHERNET
1 = ENABLE ETHERNET
0 = DISABLE USB HOST
1 = ENABLE USB HOST
00 = USB INTERRUPT DISABLED
XX = USB INTERRUPT PRIORITY
00 = WIFI INTERRUPT DISABLED
XX = WIFI INTERRUPT PRIORITY

Timer A

TIMER A CONTROL/STATUS REGISTER / TACSR (0x00A0)

(WRITE)
0 = CORRESPONDING TIMER A INTERRUPT IS DISABLED
1 = CORRESPONDING TIMER A INTERRUPT IS ENABLED
(READ)
0 = CORRESPONDING TIMER A HAS NOT REACHED TERM. COUNT
1 = CORRESPONDING TIMER A HAS REACHED TERM. COUNT
0 = TIMER A CLOCK IS DISABLED
1 = TIMER A CLOCK IS ENABLED

TIMER A PRESCALE REGISTER / TAPR (0x00A1)

TIMER A CLOCK DIVIDER

RESULTS IN ALL TIMER A TIMERS TO BE CLOCKED BY PCLK OR PCLK/2

TIMER A CONSTANT REGISTER / TACR (0x00A4)

0 = CORRESPONDING TIMER A CLK IS DISABLED
1 = CORRESPONDING TIMER A CLK IS ENABLED
00 = INTERRUPTS DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

TIMER CONSTANT REGISTERS

TIMER	CASCADE FROM	PERIPHERAL
TAT1R (0x00A3)	NONE	VARIOUS
TAT2R (0x00A5)	A1	SERIAL PORT E
TAT3R (0x00A7)	A1	SERIAL PORT F
TAT4R (0x00A9)	A1	SERIAL PORT G
TAT5R (0x00AB)	A1	SERIAL PORT B
TAT6R (0x00AD)	A1	SERIAL PORT D
TAT7R (0x00AF)	A12	INPUT CAPTURE
TAT8R (0x00B1)	A12	PWM
TAT9R (0x00B3)	A12	QUADRATURE DECODER
TAT10R (0x00AC)	A12	TIMERS B AND C
TAT12R (0x00AE)	NONE	TIMERS AA A11

Quadrature Decoder

(USES TIMER A10)

QUAD DECODE CONTROL REGISTER
QDCR (0x0091)

00 = QD2 DISABLED
01 = QD2 FROM PE0 & PE2
10 = QD2 FROM PE3 & PE2
11 = QD2 FROM PE7 & PE6
0 = 8-BIT COUNTER
1 = 16-BIT COUNTER
00 = QD1 DISABLED
01 = QD1 FROM PD0 & PD2
10 = QD1 FROM PE1 & PE3
11 = QD1 FROM PE5 & PE4
00 = QD INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

QUAD DECODE CONTROL/STATUS REGISTER
QDCSR (0x0090)

1 = QD2 = INCREMENTED FROM MAX=> 0x00
1 = QD2 = DECREMENTED FROM 0x00=> MAX
RESET QD2, NO INTERRUPT
1 = QD1 = INCREMENTED FROM MAX=> 0x00
1 = QD1 = DECREMENTED FROM 0x00=> MAX
RESET QD1, NO INTERRUPT

QUAD DECODE COUNT REGISTER
QDCNTR (0x0096) QDC2NR (0x0096)

BITS 0-7 OF QD COUNT

QUAD DECODE HIGH COUNT REGISTER
QDC1HR (0x0095) QDC2HR (0x0097)

BITS 8-9 OF QD COUNT

Breakpoints

BREAKPOINT CONTROL REGISTER
B0CR (0x0308) B4CR (0x034B)
B1CR (0x031B) B5CR (0x036B)
B2CR (0x0328) B6CR (0x0378)
B3CR (0x0338) B7CR (0x0388)
00 = NO BKPT ON EXECUTE MATCH
01 = BKPT ON USER EXECUTE MATCH
10 = BKPT ON SYSTEM EXECUTE MATCH
11 = BKPT ON SYS OR USER EXECUTE MATCH
00 = NO BKPT ON WRITE MATCH
01 = BKPT ON USER WRITE MATCH
10 = BKPT ON SYSTEM WRITE MATCH
11 = BKPT ON SYS OR USER WRITE MATCH
RESERVED MUST = 0

BREAKPOINT ADDRESS REGISTERS

B0AR (0x030E)	B0A1R (0x030D)	B0A0R (0x030C)
B1AR (0x031E)	B1A1R (0x031D)	B1A0R (0x031C)
B2AR (0x032E)	B2A1R (0x032D)	B2A0R (0x032C)
B3AR (0x033E)	B3A1R (0x033D)	B3A0R (0x033C)
B4AR (0x034E)	B4A1R (0x034D)	B4A0R (0x034C)
B5AR (0x036E)	B5A1R (0x036D)	B5A0R (0x036C)
B6AR (0x037E)	B6A1R (0x037D)	B6A0R (0x037C)
B7AR (0x038E)	B7A1R (0x038D)	B7A0R (0x038C)

PHYSICAL ADDRESS MASK

BREAKPOINT MASK REGISTERS

B0MR2R (0x030A)	B0MR1R (0x0309)	B0MR0R (0x0308)
B1MR2R (0x031A)	B1MR1R (0x0319)	B1MR0R (0x0318)
B2MR2R (0x032A)	B2MR1R (0x0329)	B2MR0R (0x0328)
B3MR2R (0x033A)	B3MR1R (0x0339)	B3MR0R (0x0338)
B4MR2R (0x034A)	B4MR1R (0x0349)	B4MR0R (0x0348)
B5MR2R (0x036A)	B5MR1R (0x0369)	B5MR0R (0x0368)
B6MR2R (0x037A)	B6MR1R (0x0379)	B6MR0R (0x0378)
B7MR2R (0x038A)	B7MR1R (0x0389)	B7MR0R (0x0388)

PHYSICAL ADDRESS MASK

BREAKPOINT/DEBUG CONTROL REGISTER
BDCR (0x001C)

0 = NORMAL RST28
1 = RST28 = NOP
RD = CORRESPONDING BREAKPOINT IS PENDING, CLEARED WHEN THIS REGISTER READ
WR = MAKE CORRESPONDING BREAKPOINT PENDING

Tamper-Protect RAM

TAMPER –PROTECT BYTE X

VRAM00 (0x0600)	VRAM08 (0x0608)	VRAM16 (0x0610)	VRAM24 (0x0618)
VRAM01 (0x0601)	VRAM09 (0x0609)	VRAM17 (0x0611)	VRAM25 (0x0619)
VRAM02 (0x0602)	VRAM10 (0x060A)	VRAM18 (0x0612)	VRAM26 (0x061A)
VRAM03 (0x0603)	VRAM11 (0x060B)	VRAM19 (0x0613)	VRAM27 (0x061B)
VRAM04 (0x0604)	VRAM12 (0x060C)	VRAM20 (0x0614)	VRAM28 (0x061C)
VRAM05 (0x0605)	VRAM13 (0x060D)	VRAM21 (0x0615)	VRAM29 (0x061D)
VRAM06 (0x0606)	VRAM14 (0x060E)	VRAM22 (0x0616)	VRAM30 (0x061E)
VRAM07 (0x0607)	VRAM15 (0x060F)	VRAM23 (0x0617)	VRAM31 (0x061F)

ACCESS TAMPER-PROTECTED BYTE

Stack Limit Protection

STACK LIMIT CONTROL REGISTER
STKCR (0x0444)

0 = DISABLE STACK LIMIT CHECKING
1 = ENABLE STACK LIMIT CHECKING

STACK LOW LIMIT REGISTER
STKLLR (0x445)

SET LOWER LIMIT FOR STACK LIMIT CHECKING

IF STACK ACCESS ATTEMPTED BELOW STKLLR, 0x10 INTERRUPT OCCURS

STACK HIGH LIMIT REGISTER
STKHLR (0x0446)

SET UPPER LIMIT FOR STACK LIMIT CHECKING

IF STACK ACCESS ATTEMPTED ABOVE (STKHLR; 0x00EF) INTERRUPT OCCURS

Watchdog Timer

WATCHDOG TIMER CONTROL REGISTER
WDTCR (0x0008)

0x5A = RESET WDT WITH 2-SECOND TIMEOUT
0x57 = RESET WDT WITH 1-SECOND TIMEOUT
0x59 = RESET WDT WITH 0.5-SECOND TIMEOUT
0x53 = RESET WDT WITH 0.25-SECOND TIMEOUT
0x1E = ENABLE SECONDARY WATCHDOG TIMER
OTHER = NO EFFECT
READ = LSB OF CPU CLOCK CYCLE COUNTER

WATCHDOG TIMER TEST REGISTER
WDTTR (0x0009)

0x54 = DISABLE WDT (MUST BE PRECEDED BY A WRITE OF 0x51,0x52, OR 0x53)
OTHER = NORMAL WATCHDOG TIMER
READ = MSB OF CPU CLOCK CYCLE COUNTER

SECONDARY WATCHDOG TIMER
SWDTB (0x0002)

SECONDARY WATCHDOG TIMER TIME CONSTANT DISABLED IF 0x3A - 0x52 - 0x44 TO THIS REGISTER

Real-Time Clock

REAL-TIME CLOCK x REGISTER

RTC0R (0x0002) R/W
RTC1R (0x0003) RD
RTC2R (0x0004) RD
RTC3R (0x0005) RD
RTC4R (0x0006) RD
RTC5R (0x0007) RD

RD = CURRENT VALUE OF 48-BIT RTC HOLDING REGISTER
W = A WRITE TO RTC0R TRANSFERS CURRENT COUNT OF RTC TO HOLDING REGISTER

REAL-TIME CLOCK CONTROL REGISTER
RTCCR (0x0001)

0 = THIS BIT COMBINATION MUST BE USED WITH EVERY BYTE INCREMENT WRITE
0 = NO EFFECT ON RTC COUNTER
1 = INCREMENT CORRESPONDING BYTE OF RTC (RTCxB)

RTCCR (SHORTCUTS)

0x00 = NO EFFECT ON RTC COUNTER DISABLE BYTE INCREMENT CANCEL RTC COMMAND
0x40 = ARM RTC FOR RESET ON BYTE INCREMENT. BYTE INCREMENT MUST BE WRITTEN PRIOR TO RTC RESET ON FIRST BYTE RESET
0x80 = RESET ALL SIX BYTES OF RTC TO 0x00, RESET MUST BE PRECEDED BY WRITING 0x40 TO ARM RESET FUNCTION
0xC0 = RESET ALL SIX BYTES IN RTC COUNTER TO 0x00 AND REMAIN IN BYTE INCREMENT MODE

External I/O

I/O BANK x CONTROL REGISTER

I/O ADDRESS	I/O BANK	CONTROL REGISTER	PORT SIGNAL	EXTENDED REGISTER
xx xx HH				
1 1 1	IB7CR	(0x0087)	I7	(0x045F)
1 1 0	IB6CR	(0x0086)	I6	(0x045D)
1 0 1	IB5CR	(0x0085)	I5	(0x045B)
1 0 0	IB4CR	(0x0084)	I4	(0x0459)
0 1 1	IB3CR	(0x0083)	I3	(0x0457)
0 1 0	IB2CR	(0x0082)	I2	(0x0455)
0 0 1	IB1CR	(0x0081)	I1	(0x0453)
0 0 0	IB0CR	(0x0080)	I0	(0x0451)

WAITS STATES
00 = 15 WS
01 = 7 WS
10 = 3 WS
11 = 1 WS
I/O STROBE FUNCTIONS (IX)
000 = I/O /CS
001 = I/O /RD STROBE
010 = I/O /WR STROBE
011 = I/O DATA (/RD OR /WR) STROBE
100 = WRITES NOT ALLOWED
111 = WRITES ALLOWED
0 = ACTIVE LOW STROBE
1 = ACTIVE HIGH STROBE
0 = NORMAL I/O TRANSACTION TIMING
1 = SHORTEN READ/WRITE STROBES
0 = USE I/O BUS IF ENABLED
1 = ALWAYS USE MEMORY DATA BUS

I/O BANK x EXTENDED REGISTER

0 = I/O BANK IS 8-BIT
1 = I/O BANK IS 16-BIT

**I/O HANDSHAKE T