RABBIT® 4000 MICROPROCESSOR

REFERENCE

REGISTER LEGEND

Read/Write | Write Only | Read Only | Read (Special Behavior on Write Operation)

NOTE: ZERO MUST BE WRITTEN TO ALL UNUSED BITS

Processor Control

GLOBAL CLOCK MODULATOR REGISTERS
GCM0R (0x0A) — GCM1R (0x0B)

GCM0R: 00 = 1 ns SPREADING; 01 = 0.25 ns SPREADING; 10 = 0.5 ns SPREADING; RESERVED MUST = 0
GCM1R: 0 = SPREADER OFF; 1 = SPREADER ON; RESERVED MUST = 0

GLOBAL CONTROL/STATUS REGISTER
GCSR (0x00)

RD ONLY
00 = NO RESET OR WD TIMEOUT
01 = WATCHDOG TIMEOUT
10 = NOT POSSIBLE
11 = RESET OCCURRED
WRITE 1 = FORCE A PERIODIC INTERRUPT TO BE PENDING
OSC
000 CPU = OSC/8; PCLK = OSC/8
001 CPU = OSC/8; PCLK = OSC
010 CPU = OSC; PCLK = OSC
011 CPU = OSC/2; PCLK = OSC/2
100 CPU = 32 kHz; PCLK = 32 kHz; MAIN OSC ON
101 CPU = 32 kHz; PCLK = 32 kHz; MAIN OSC OFF
110 CPU = OSC/4; PCLK = OSC/4
111 CPU = OSC/6; PCLK = OSC/6
PERIODIC INTERRUPT
00 PERIODIC INTERRUPT = DISABLE
01 PERIODIC INTERRUPT = PRIORITY 1
10 PERIODIC INTERRUPT = PRIORITY 2
11 PERIODIC INTERRUPT = PRIORITY 3
PERIODIC INTERRUPT = 32 kHz/16 (488 ms)
PCLK = PERIPHERAL CLOCK
CPU = CPU CLOCK
OSC = DOUBLED OR NON DOUBLED CLOCK

GLOBAL OUTPUT CONTROL REGISTER
GOCR (0x0E)

CLK OUTPUT
00 = CLK = PCLK
01 = CLK = PCLK/2
10 = CLK = LOW
11 = CLK = HIGH
STATUS OUTPUT
00 = LOW DURING FIRST OPCODE FETCH
01 = LOW DURING INTERRUPT ACKNOWLEDGE
10 = LOW
11 = HIGH
/WDTOUT OUTPUT — 0 = LOW DURING WATCHDOG TIMEOUT (30.5 ms); 1 = LOW PULSE FOR DURATION OF 30.5 – 61 ms
/BUFEN OUTPUT
00 = LOW FOR EXTERNAL I/O CYCLE
01 = LOW FOR DATA MEMORY CYCLE
10 = LOW
11 = HIGH

GLOBAL POWER SAVE CONTROL REGISTER
GPSCR (0x0D)

000 = SELF-TIMED CS DISABLE
001 = 230 ns
010 = 170 ns
011 = 110 ns — SELF-TIMED CS READ ONLY
100 = 290 ns
101 = 230 ns
110 = 170 ns
111 = 110 ns — SELF-TIMED CS READ AND WRITE
0 = NORMAL CS FOR READS
1 = SHORT CS TIMING FOR READS
0 = NORMAL CS FOR WRITES
1 = SHORT CS TIMING FOR WRITES
000 = 32 kHz
001, 01X = RESERVED
100 = 16.3848 kHz
101 = 8.192 kHz
110 = 4.096 kHz
111 = 2.048 kHz — CPU & PCLK
#(NOT AVAILABLE AT FULL SPEED)

GLOBAL CLOCK DOUBLE REGISTER
GCDR (0x0F)

RESERVED MUST = 0
00000 = CLOCK DOUBLE DISABLED
00001 6 ns
00010 7 ns
00011 8 ns
00100 9 ns
00101 10 ns
00110 11 ns
00111 12 ns
01000 13 ns
01001 14 ns
01010 15 ns
01011 16 ns
01100 17 ns
01101 18 ns
01110 19 ns
01111 20 ns
10001 3 ns
10010 4 ns
10011 5 ns
TYPICAL DOUBLED CLOCK LOW TIME

GLOBAL CPU CONFIGURATION REGISTER
GCPU (0x2E)
GLOBAL REVISION REGISTER
GREV (0x2F)

0 = FETCH PER SMODE; 1 = IGNORE SMODE — RD ONLY
SMODE
CPU VERSION (GCPU) REVISION (GREV)

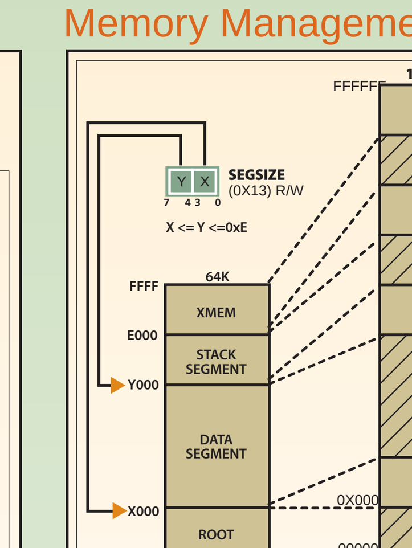
PROCESSOR MODE SELECT

SMODE1	SMODE0	BOOTSTRAP OPERATION
0	0	BOOTSTRAP DISABLED. NORMAL PROCESSOR OPERATION(CODE FETCHED FROM MEMORY)
0	1	SLAVE PORT. SPD0R USED FOR BOOTSTRAP OPERATION
1	0	SYNCHRONOUS SERIAL. CLOCKED SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. MAX EXTERNAL CLOCK RATE = PCLK/6
1	1	ASYNCHRONOUS SERIAL. ASYNCH SERIAL PORT A ON PARALLEL PORT C USED FOR BOOTSTRAP OPER. REQUIRED BAUD RATE = 2400

REVISION IDENTIFIERS

	Marking	CPU	Revision
RABBIT 4000LQFP	UL1T	0x02	0x00
RABBIT 4000BGA	JCT1T	0x02	0x00

Memory Management Unit



SEGMENT H/L — SEGMENT REGISTERS
+ 16-BIT LOGICAL ADDRESS
24-BIT PHYSICAL ADDRESS

LXPC / 0000 XPC — EXTENDED PROGRAM COUNTER REGISTER

DATASEG H/L — DATA SEGMENT H/L REGISTERS (0x1E) (0x1F)
STACKSEG H/L — STACK SEGMENT H/L REGISTERS (0x18) (0x1A)
0000 DATASEG — DATA SEGMENT REGISTER (0x12) R/W
0000 STACKSEG — STACK SEGMENT REGISTER (0x11) R/W

WRITING TO DATASEG/STACKSEG PUTS 8-BIT VALUE INTO DATASEGL/STACKSEGL AND 0000 INTO DATASEGH/STACKSEGH.

WRITING TO XPC PUTS VALUE INTO LOWER 8 BITS AND 0000 INTO UPPER 4 BITS OF LXPC

MEMORY BANK CONTROL REGISTERS

A[19:18]	CONTROL REGISTER USED	ADDRESS
00	MB0CR	(0x14) W
01	MB1CR	(0x15) W
10	MB2CR	(0x16) W
11	MB3CR	(0x17) W

MBxCR
00 = 4 WS (5 FOR WRITES)
01 = 2 WS (3 FOR WRITES)
10 = 1 WS (2 FOR WRITES)
11 = 0 WS (1 FOR WRITES)
0 = PASS MSB
1 = INVERT MSB
0 = PASS LSB
1 = INVERT LSB BANKSEL ADDR (ALL FOUR)
00 = USE /OE0 & /WE0
01 = USE /OE1 & /WE1
10 = USE /OE0 (READ ONLY)
11 = USE /OE1 (READ ONLY)
00 = USE /CS0
01 = USE /CS1
10 = USE /CS2

ADVANCED CHIP SELECT CONTROL REGISTERS
ACS0R (0x410) ACS1R (0x411)

000 = 7 WS 16-BIT / 1ST PAGE READ
001 = 6 WS 16-BIT / 1ST PAGE READ
010 = 5 WS 16-BIT / 1ST PAGE READ
011 = 4 WS 16-BIT / 1ST PAGE READ
100 = 3 WS 16-BIT / 1ST PAGE READ
101 = 2 WS 16-BIT / 1ST PAGE READ
110 = 1 WS 16-BIT / 1ST PAGE READ
111 = RESERVED
00 = 3 WS FOR LATER PAGE READS
01 = 2 WS FOR LATER PAGE READS
10 = 1 WS FOR LATER PAGE READS
11 = 0 WS FOR LATER PAGE READS
000 = 9 (7 BASIC) WS FOR 16-BIT WRITE
001 = 8 (6) WS FOR 16-BIT WRITE
010 = 7 (5) WS FOR 16-BIT WRITE
011 = 6 (4) WS FOR 16-BIT WRITE
100 = 5 (3) WS FOR 16-BIT WRITE
101 = 4 (2) WS FOR 16-BIT WRITE
110 = 3 (1) WS FOR 16-BIT WRITE
111 = RESERVED

RAM SEGMENT REGISTER
RAMSR (0X448)

COMPARE VALUE FOR DATA MMU TRANSLATION WINDOW
00 = DISABLE RAM SEGMENT LIMIT CHECKING
01 = SELECT DATA MMU TRANSLATION IF PC[15:10] = RAMSR[7:2]
10 = SELECT DATA MMU TRANSLATION IF PC[15:11] = RAMSR[7:3]
11 = SELECT DATA MMU TRANSLATION IF PC[15:12] = RAMSR[7:4]

MMU INSTRUCTION/DATA REGISTER
MMIDR (0x10) R/W

0 = USE 8-BIT INTERNAL I/O ADDRESSES
1 = USE 15-BIT INTERNAL I/O ADDRESSES
RESERVED WRITE MUST = 0
0 = A16, MSB INVERSION INDEPENDENT OF INSTRUCTION/DATA
1 = A16, MSB INVERSION FOR DATA ACCESS ONLY. (THIS ENABLES SEPARATE I AND D SPACE)
0 = NORMAL /CS1 OPERATION
1 = FORCE /CS1 ALWAYS ACTIVE
0 = NORMAL
1 = INVERT MSB ON DATASEG ACCESS
0 = NORMAL
1 = INVERT A16 ON DATASEG ACCESS
0 = NORMAL
1 = INVERT MSB ON ROOT ACCESS
0 = NORMAL
1 = INVERT A16 ON ROOT ACCESS

MMU EXPANDED CODE REGISTER
MECR (0x18)

000 = BANK SELECT ADDRESS IS A [19:18]
001 = BANK SELECT ADDRESS IS A [20:19]
010 = BANK SELECT ADDRESS IS A [21:20]
011 = BANK SELECT ADDRESS IS A [22:21]
100 = BANK SELECT ADDRESS IS A [23:22]
111 = BANK SELECT ADDRESS IS A [18:17]
OTHERS RESERVED
000 = NORMAL
100 = USE MB0CR FOR XPC ACCESS
101 = USE MB1CR FOR XPC ACCESS
110 = USE MB2CR FOR XPC ACCESS
111 = USE MB3CR FOR XPC ACCESS
OTHERS RESERVED

MEMORY ALTERNATE CONTROL REGISTER
MACR (0x001D)

00 = 8-BIT OPERATION FOR /CS1
01 = ADVANCED 16-BIT OPERATION FOR /CS1 (NO BYTE WRITE)
10 = BASIC 16-BIT OPERATION FOR /CS1
11 = ADVANCED 16-BIT OPERATION FOR /CS1 (BYTE WRITE)
0 = PAGE-MODE DISABLED FOR /CS1
1 = PAGE-MODE ENABLED FOR /CS1
00 = 8-BIT OPERATION FOR /CS0
01 = ADVANCED 16-BIT OPERATION FOR /CS0 (NO BYTE WRITE)
10 = BASIC 16-BIT OPEARTION FOR /CS0
11 = ADVANCED 16-BIT OPERATION FOR /CS0 (BYTE WRTIE)
0 = PAGE-MODE DISABLED FOR /CS0
1 = PAGE-MODE ENABLED FOR /CS0

MEMORY TIMING CONTROL REGISTER
MTCR (0x19) W

0 0 0 0 /OE1 /OE0 /WE1 /WE0
RESERVED MUST = 0
0 = NORMAL TIMING FOR
1 = EXTENDED TIMING FOR

Timer A

TIMER A CONTROL/STATUS REGISTER / TACSR (0xA0)

TMRA7 TMRA6 TMRA5 TMRA4 TMRA3 TMRA2 TMRA1
(WRITE)
0 = CORRESPONDING TIMER A INTERRUPT IS DISABLED
1 = CORRESPONDING TIMER A INTERRUPT IS ENABLED
0 = MAIN CLOCK FOR TIMER A DISABLED
1 = MAIN CLOCK FOR TIMER A ENABLED
(READ)
0 = CORRESPONDING TIMER A HAS NOT REACHED TERM. COUNT
1 = CORRESPONDING TIMER A HAS REACHED TERM. COUNT

TIMER A PRESCALE REGISTER / TAPR (0xA1)

0 0 0 0 0 0 0
RESERVED MUST = 0
0 = CLOCK = PCLK
1 = CLOCK = PCLK/2
RESULTS IN ALL TIMER A TIMERS TO BE CLOCKED BY PCLK OR PCLK/2

TIMER A CONTROL REGISTER / TACR (0xA4)

TMRA7 TMRA6 TMRA5 TMRA4 TMRA3 TMRA2
0 = CORRESPONDING TIMER CLOCKED BY MAIN TIMER A CLK
1 = CORRESPONDING TIMER CLOCKED BY TIMER A1
00 = INTERRUPTS DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

PCLK or PCLK/2 → TIMER A1 → TIMER A2: TMRA2 OUT, SERIAL E BAUD CLOCK; TIMER A3: TMRA3 OUT, SERIAL F BAUD CLOCK; TIMER A4: TMRA4 OUT, SERIAL A BAUD CLOCK; TIMER A5: TMRA5 OUT, SERIAL B BAUD CLOCK; TIMER A6: TMRA6 OUT, SERIAL C BAUD CLOCK; TIMER A7: TMRA7 OUT, SERIAL D BAUD CLOCK

TIME CONSTANT REGISTER

TAT1R	(0xA3)
TAT2R	(0xA5)
TAT3R	(0xA7)
TAT4R	(0xA9)
TAT5R	(0xAB)
TAT6R	(0xAD)
TAT7R	(0xAF)
TAT8R	(0xA6) INPUT CAPTURE
TAT9R	(0xA8) PWM
TAT10R	(0xAA) QUAD DECODER

Timer B

TIMER B CONTROL/STATUS REGISTER
TBCSR (0xB0)

0 0 0 0 0
(WRITE)
0 = CORRESPONDING INTERRUPT IS DISABLED
1 = CORRESPONDING INTERRUPT IN ENABLED
0 = MAIN CLOCK IS DISABLED
1 = MAIN CLOCK IS ENABLED
(READ)
0 = CORRESPONDING HAS NOT ENCOUNTERED A MATCH
1 = CORRESPONDING INT. HAS ENCOUNTERED A MATCH (STATUS BITS AND INTERUPTS ARE CLEARED BY READ OF THIS REGISTER)

TIMER B CONTROL REGISTER
TBCR (0xB1)

BITS [7:6] IGNORED
0 = NORMAL B2 OPERATION
1 = B2 USES STEP REGS
0 = NORMAL B1 OPERATION
1 = B1 USES STEP REGS
00 = CLOCKED BY PCLK/2
01 = CLOCKED BY TIMER A1
1X = CLOCKED BY PCLK/16
00 = INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

TIMER B MATCH 1 REGISTER
(MSByte) BIT9 BIT8 0 0 0 0 0 0 — TBM1R (0xB2)
(LSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBL1R (0xB3)

TIMER B MATCH 2 REGISTER
(MSByte) BIT9 BIT8 0 0 0 0 0 0 — TBM2R (0xB4)
(LSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBL2R (0xB5)

TIMER B COUNT REGISTER
(MSByte) BIT9 BIT8 0 0 0 0 0 0 — TBCMR (0xBE)
(LSByte) BIT7 BIT6 BIT5 BIT4 BIT3 BIT2 BIT1 BIT0 — TBCLR (0xBF)

TIMER B STEP LSB x REGISTER
TBSL1R (0x00BA) TBSL2R (0x00BC)
LSB OF STEP SIZE FOR COMPARATOR

TIMER B STEP MSB x REGISTER
TBSM1R (0x00BB) TBSM2R (0x00BD)
0 0 0 0 0 0
MSB OF STEP SIZE FOR COMPARATOR

Timer C

TIMER C CONTROL/STATUS REGISTER
TCCSR (0x0500)

0 0 0 0 0 0
0 = LIMIT NOT REACHED
1 = LIMIT REACHED
0 = MAIN CLOCK IS DISABLED
1 = MAIN CLOCK IS ENABLED

TIMER C CONTROL REGISTER
TCCR (0x0501)

0 0 0 0
00 = CLOCKED BY PCLK/2
01 = CLOCKED BY TIMER A1
10 = CLOCKED BY PCLK/16
11 = CLOCKED BY PCLK/16
00 = INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

TIMER C RESET x LOW REGISTER / **TIMER C RESET x HIGH REGISTER**
TCR0LR (0x050A) TCR1LR (0x050E) TCR0HR (0x050B) TCR1HR (0x050F)
TCR2LR (0x051A) TCR3LR (0x051E) TCR2HR (0x051B) TCR3HR (0x051F)

TIMER C SET x LOW REGISTER / **TIMER C SET x HIGH REGISTER**
TCS0LR (0x0508) TCS1LR (0x050C) TCS0HR (0x0509) TCS1HR (0x050D)
TCS2LR (0x0518) TCS3LR (0x051C) TCS2HR (0x0519) TCS3HR (0x051D)

TIMER C DIVIDER LOW REGISTER
TCDLR (0x0502)
TIMER C DIVIDER HIGH REGISTER
TCDHR (0x0503)

TIMER C BLOCK ACCESS REGISTER
TCBAR (0x00F8)
ACCESS REGISTER POINTED BY TCBPR

TIMER C BLOCK POINTER REGISTER
TCDBPR (0x00F9)
0 0 0
LSB OF REGISTER ADDRESS

Direct Memory Access

DMA MASTER CONTROL/STATUS REGISTER
DMCSR (0x0100)

WR 0=NO EFFECT
WR 1=START/RESTART CHANNEL
RD 0=CHANNEL DISABLED
RD 1=CHANNEL ENABLED

DMA MASTER TIMING CONTROL REGISTER
DMTCR (0x0105)

0x = FIXED PRIORITY
10 = ROTATE PRIORITY AFTER EVERY BYTE TRANSFER
11 = ROTATE PRIORITY AFTER EVERY REQUEST IS SERVICED
000 = MAX 1 BYTE BURST
001 = MAX 2 BYTE BURST
010 = MAX 3 BYTE BURST
011 = MAX 4 BYTE BURST
100 = MAX 8 BYTE BURST
101 = MAX 16 BYTE BURST
110 = MAX 32 BYTE BURST
111 = MAX 64 BYTE BURST
000 = MIN 12 CLOCKS BETWEEN BURSTS
001 = MIN 16 CLOCKS BETWEEN BURSTS
010 = MIN 24 CLOCKS BETWEEN BURSTS
011 = MIN 32 CLOCKS BETWEEN BURSTS
100 = MIN 64 CLOCKS BETWEEN BURSTS
101 = MIN 128 CLOCKS BETWEEN BURSTS
110 = MIN 256 CLOCKS BETWEEN BURSTS
111 = MIN 512 CLOCKS BETWEEN BURSTS

DMA x BUFFER COMPLETE REGISTER
D0BCR (0x0103) D1BCR (0x0113) D2BCR (0x0123) D3BCR (0x0133) D4BCR (0x0143) D5BCR (0x0153) D6BCR (0x0163) D7BCR (0x0173)
WR = LOAD COUNTER
RD = READ COUNTER

DMA MASTER CONTROL REGISTER
DMCR (0x0104)

00 = DISABLE INTERRUPT
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT
00 = PRIORITY 0 TRANSFER
01 = PRIORITY 1 TRANSFER
10 = PRIORITY 2 TRANSFER
11 = PRIORITY 3 TRANSFER

DMA x BUFFER UNUSED [7:0] REGISTER
D0BU0R (0x010A) D1BU0R (0x011A)
D2BU0R (0x012A) D3BU0R (0x013A)
D4BU0R (0x014A) D5BU0R (0x015A)
D6BU0R (0x016A) D7BU0R (0x017A)

DMA x BUFFER UNUSED [15:8] REGISTER
D0BU1R (0x010B) D1BU1R (0x011B)
D2BU1R (0x012B) D3BU1R (0x013B)
D4BU1R (0x014B) D5BU1R (0x015B)
D6BU1R (0x016B) D7BU1R (0x017B)
STORES BITS OF BUFFER UNUSED LENGTH VALUE

DMA x TERMINATION BYTE REGISTER
D0TBR (0x0108) D1TBR (0x0118)
D2TBR (0x0128) D3TBR (0x0138)
D4TBR (0x0148) D5TBR (0x0158)
D6TBR (0x0168) D7TBR (0x0178)
MATCH VALUE

DMA x TERMINATION MASK REGISTER
D0TMR (0x0109) D1TMR (0x0119)
D2TMR (0x0129) D3TMR (0x0139)
D4TMR (0x0149) D5TMR (0x0159)
D6TMR (0x0169) D7TMR (0x0179)
TERMINATION BYTE MASK

DMA x STATE MACHINE REGISTER
D0SMR (0x0180) D1SMR (0x0190)
D2SMR (0x01A0) D3SMR (0x01B0)
D4SMR (0x01C0) D5SMR (0x01D0)
D6SMR (0x01E0) D7SMR (0x01F0)
REFER TO MANUAL FOR DETAILS

DMA MASTER REQUEST 0 COUNTER REGISTER
DMR0CR (0x0106)

00 = REQUESTS DISABLED
01 = REQUEST ENABLED FROM PD2
10 = REQUEST ENABLED FROM PE2
11 = REQUEST ENABLED FROM PE6
00 = FALLING EDGE TRIGGERED (1 BYTE)
01 = RISING EDGE TRIGGERED (1 BYTE)
10 = ACTIVE LOW
11 = ACTIVE HIGH
000 = REQUEST TO CHANNEL 0
001 = REQUEST TO CHANNEL 1
010 = REQUEST TO CHANNEL 2
011 = REQUEST TO CHANNEL 3
100 = REQUEST TO CHANNEL 4
101 = REQUEST TO CHANNEL 5
110 = REQUEST TO CHANNEL 6
111 = REQUEST TO CHANNEL 7

DMA MASTER REQUEST 1 CONTROLREGISTER
DMR1CR (0X0107)

00 = REQUESTS DISABLED
01 = REQUEST ENABLED FROM PD3
10 = REQUEST ENABLED FROM PE3
11 = REQUEST ENABLED FROM PE7
00 = FALLING EDGE TRIGGERED (1 BYTE)
01 = RISING EDGE TRIGGERED (1 BYTE)
10 = ACTIVE LOW
11 = ACTIVE HIGH
000 = REQUEST TO CHANNEL 0
001 = REQUEST TO CHANNEL 1
010 = REQUEST TO CHANNEL 2
011 = REQUEST TO CHANNEL 3
100 = REQUEST TO CHANNEL 4
101 = REQUEST TO CHANNEL 5
110 = REQUEST TO CHANNEL 6
111 = REQUEST TO CHANNEL 7

DMA MASTER AUTO-LOAD REGISTER
DMALR (0X0101)
0 = NO EFFECT
1 = AUTO-LOAD CHANNEL

DMA MASTER HALT REGISTER
DMHR (0x0102)
0 = NO EFFECT
1 = HALT CHANNEL

DMA TIMED REQUEST CONTROL REGISTER
DTRCR (0x0115)

0 = TIMED REQUEST DISABLED
1 = TIMED REQUEST ENABLED
00 = 1 BYTE PER REQUEST
01 = (RESERVED)
10 = TRANSFER UNTIL DISCRIPTOR IS COMPLETE
11 = (RESERVED)
000 = REQUEST TO CHANNEL 0
001 = REQUEST TO CHANNEL 1
010 = REQUEST TO CHANNEL 2
011 = REQUEST TO CHANNEL 3
100 = REQUEST TO CHANNEL 4
101 = REQUEST TO CHANNEL 5
110 = REQUEST TO CHANNEL 6
111 = REQUEST TO CHANNEL 7

DMA TIMED REQUEST DIVIDER HIGH REGISTER
DTRDHR (0x0117)
MSB OF LIMIT VALUE FOR TIMER

DMA TIMED REQUEST DIVIDER LOW REGISTER
DTRDLR (0x0116)
LSB OF LIMIT VALUE FOR TIMER

DMA DESCRIPTOR REGISTER
- CHANNEL 0 ADDRESSING SHOWN. ADD MULTIPLE OF 16 FOR CHANNELS 1 THRU 7 -

D0CR (0x0181): (0x181) → SEE BIT SETTINGS BELOW
D0L0R (0x0182): (0x183) (0x182) — DMA LENGTH REG
D0SA0R (0x0184): (0x0186) (0x0185) (0x0184) — DMA SOURCE ADDRESS
D0DA0R (0x0188): (0x018A) (0x0189) (0x188) — DMA DEST ADDRESS
D0LA0R (0x0180): (0x018E) (0x018D) (0x18C) — DMA LINK ADDRESS

DMA x CONTROL REGISTER
D0CR (0x0181)

0 = CONTINUE TO NEXT DESCRIPTOR
1 = FINAL DESCRIPTOR
0 = USE SEQUENTIAL ADDRESS
1 = USE LINK ADDRESS FIELD
0 = NORMAL
1 = SPECIAL LAST BYTE
0 = NO INTERRUPT ON COMPLETION
1 = INTERRUPT ON COMPLETION
00 = SOURCE ADDRESS IS FIXED INTERNAL I/O ADDRESS
01 = SOURCE ADDRESS IS FIXED EXTERNAL I/O ADDRESS
10 = SOURCE ADDRESS IS MEMORY ADDR, AUTO-DECREMENT
11 = SOURCE ADDRESS IS MEMORY ADDR, AUTO-INCREMENT
00 = DESTINATION ADDRESS IS FIXED INTERNAL I/O ADDR
01 = DESTINATION ADDRESS IS FIXED EXTERNAL I/O ADDR
10 = DESTINATION ADDRESS IS MEMORY ADDR, AUTO DECREMENT
11 = DESTINATION ADDRESS IS MEMORY ADDR, AUTO INCREMENT

External Interrupts

INTERRUPT 0 CONTROL REGISTER
I0CR (0x98)

00 = DISABLE PD0 INTERRUPT
01 = ENABLE PD0 FALLING EDGE
10 = ENABLE PD0 RISING EDGE
11 = ENABLE PD0 BOTH EDGES
00 = DISABLE PE4 INTERRUPT
01 = ENABLE PE4 FALLING EDGE
10 = ENABLE PE4 RISING EDGE
11 = ENABLE PE4 BOTH EDGES
00 = DISABLE PE0 INTERRUPT
01 = ENABLE PE0 FALLING EDGE
10 = ENABLE PE0 RISING EDGE
11 = ENABLE PE0 BOTH EDGES
00 INT0 DISABLED
01 INT0 PRIORITY 1
10 INT0 PRIORITY 2
11 INT0 PRIORITY 3

INTERRUPT 1 CONTROL REGISTER
I1CR (0x99)

00 = DISABLE PD1 INTERRUPT
01 = ENABLE PD1 FALLING EDGE
10 = ENABLE PD1 RISING EDGE
11 = ENABLE PD1 BOTH EDGE
00 = DISABLE PE5 INTERRUPT
01 = ENABLE PE5 FALLING EDGE
10 = ENABLE PE5 RISING EDGE
11 = ENABLE PE5 BOTH EDGE
00 = DISABLE PE1 INTERRUPT
01 = ENABLE PE1 FALLING EDGE
10 = ENABLE PE1 RISING EDGE
11 = ENABLE PE1 BOTH EDGE
00 INT1 DISABLED
01 INT1 PRIORITY 1
10 INT1 PRIORITY 2
11 INT1 PRIORITY 3

EXTERNAL INTERRUPT HOLD TIME MUST BE AT LEAST 3 PERIPHERAL CLOCK CYCLES

Breakpoints

BREAKPOINT CONTROL REGISTER
B0CR (0x30B) B4CR (0x34B)
B1CR (0x31B) B5CR (0x36B)
B2CR (0x32B) B6CR (0x37B)
B3CR (0x33B)

00 = NO BKPT ON EXECUTE MATCH
01 = BKPT ON USER EXECUTE MATCH
10 = BKPT ON SYSTEM EXECUTE MATCH
11 = BKPT ON SYS OR USER EXECUTE MATCH
00 = NO BKPT ON READ MATCH
01 = BKPT ON USER READ MATCH
10 = BKPT ON SYSTEM READ MATCH
11 = BKPT ON SYS OR USER READ MATCH
00 = NO BKPT ON WRITE MATCH
01 = BKPT ON USER WRITE MATCH
10 = BKPT ON SYSTEM WRITE MATCH
11 = BKPT ON SYS OR USER WRITE MATCH
RESERVED MUST = 0

BREAKPOINT/DEBUG CONTROL REGISTER
BDCR (0x1C)

0 = NORMAL RST28
1 = RST28 = NOP
RD = CORRESPONDING BREAKPOINT IS PENDING. CLEARED WHEN THIS REGISTER READ
WR = MAKE CORRESPONDING BREAKPOINT PENDING

BREAKPOINT ADDRESS REGISTERS

B0A2R (0x30E)	B0A1R (0x30D)	B0A0R (0x30C)
B1A2R (0x31E)	B1A1R (0x31D)	B1A0R (0x31C)
B2A2R (0x32E)	B2A1R (0x32D)	B2A0R (0x32C)
B3A2R (0x33E)	B3A1R (0x33D)	B3A0R (0x33C)
B4A2R (0x34E)	B4A1R (0x34D)	B4A0R (0x34C)
B5A2R (0x36E)	B5A1R (0x36D)	B5A0R (0x36C)
B6A2R (0x37E)	B6A1R (0x37D)	B6A0R (0x37C)

BxA2R (23–16) BxA1R (15–8) BxA0R (7–0) — PHYSICAL ADDRESS MASK

BREAKPOINT MASK REGISTERS

B0M2R (0x30A)	B0M1R (0x309)	B0M0R (0x308)
B1M2R (0x31A)	B1M1R (0x319)	B1M0R (0x318)
B2M2R (0x32A)	B2M1R (0x329)	B2M0R (0x328)
B3M2R (0x33A)	B3M1R (0x339)	B3M0R (0x338)
B4M2R (0x34A)	B4M1R (0x349)	B4M0R (0x348)
B5M2R (0x36A)	B5M1R (0x369)	B5M0R (0x368)
B6M2R (0x37A)	B6M1R (0x379)	B6M0R (0x378)

BxA2R (23–16) BxA1R (15–8) BxA0R (7–0) — PHYSICAL ADDRESS MASK

Watchdog Timer

WATCHDOG TIMER CONTROL REGISTER
WDTCR (0x08)

0x5A = RESET WDT WITH 2 SECOND TIMEOUT
0x57 = RESET WDT WITH 1 SECOND TIMEOUT
0x59 = RESET WDT WITH 0.5 SECOND TIMEOUT
0x53 = RESET WDT WITH 0.25 SECOND TIMEOUT
0x5F = RESTART SECONDARY WATCHDOG TIMER
OTHER = NO EFFECT

WATCHDOG TIMER TEST REGISTER
WDTTR (0x09)

0x54 = DISABLE WDT (MUST BE PRECEDED BY A WRITE OF 0x51,0x52, OR 0x53) TO THIS REGISTER
OTHER = NORMAL, WATCHDOG TIMER IS CLOCKED BY 32 kHz CLOCK

SECONDARY WATCHDOG TIMER
SWDTR (0x0C)

SECONDARY WATCHDOG TIMER TIME CONSTANT DISABLED BY 0x5A - 0x52 - 0x44 TO THIS REGISTER

Pulse Width Modulation

(USES TIMER A9)

PWM 0 REGISTERS
PWM0R (0x89) PWL0R (0x88)

10 BIT PWM COUNT
00 = NORMAL PWM OPERATION
01 = SUPPRESS PWM OUTPUT 7/8 ITERATIONS
10 = SUPPRESS PWM OUTPUT 3/4 ITERATIONS
11 = SUPPRESS PWM OUTPUT 1/2 ITERATIONS
0 = SINGLE-PULSE PWM
1 = SPREAD PWM
00 = INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

PWM 1 REGISTERS
PWM1R (0x8B) PWL1R (0x8A)

10 BIT PWM COUNT
00 = NORMAL PWM OPERATION
01 = SUPPRESS PWM OUTPUT 7/8 ITERATIONS
10 = SUPPRESS PWM OUTPUT 3/4 ITERATIONS
11 = SUPPRESS PWM OUTPUT 1/2 ITERATIONS
0 = SINGLE-PULSE PWM
1 = SPREAD PWM
00 = NORMAL PWM INTERRUPT
01 = SUPPRESS PWM INT 7/8 ITERATIONS
10 = SUPPRESS PWM INT 3/4 ITERATIONS
11 = SUPPRESS PWM INT 1/2 ITERATIONS

PWM 2 AND 3 REGISTERS
PWM2R (0x8D) PWL2R (0x8C) PWM3R (0x8F) PWL3R (0x8E)

10 BIT PWM COUNT
00 = NORMAL PWM 1 OPERATION
01 = SUPPRESS PWM 1 OUTPUT 7/8 ITERATIONS
10 = SUPPRESS PWM 1 OUTPUT 3/4 ITERATIONS
11 = SUPPRESS PWM 1 OUTPUT 1/2 ITERATIONS
0 = SINGLE-PULSE PWM
1 = SPREAD PWM

PWM BLOCK ACCESS REGISTER
PWBAR (0x00E8)
ACCESS PWM REGISTER POINTED TO BY PWBPR

PWM BLOCK POINTER REGISTER
PWBPR (0x00E9)
1 0 0 0 1
LSBITS OF PWM REGISTER

Parallel Ports

PORT x DATA REGISTERS
PADR (0x30) PDDR (0x60)
PBDR (0x40) PEDR (0x70)
PCDR (0x50)
READ/WRITE DATA TO PORT

PORT x DATA DIRECTION REGISTERS
PBDDR (0x47) PDDDR (0x67)
PCDDR (0x51) PEDDR (0x77)
0 = CORRESPONDING BIT IS INPUT
1 = CORRESPONDING BIT IS OUTPUT

PORT x DRIVE CONTROL REGISTERS
PCDCR (0x54) PEDCR (0x76)
PDDCR (0x66)
0 = OUTPUT IS DRIVEN HIGH AND LOW
1 = OUTPUT IS OPEN DRAIN

PORT x FUNCTION REGISTERS
PCFR (0x55) PEFR (0x75)
PDFR (0x65)
0 = BIT FUNCTIONS AS I/O
1 = BIT IS ALTERNATE OUTPUT

PORT x CONTROL REGISTER
PDCR (0x64) PECR(0x74)

UPPER NIBBLE CLOCK IS PERCLK
UPPER NIBBLE CLOCK IS TIMER A1
UPPER NIBBLE CLOCK IS TIMER B1
UPPER NIBBLE CLOCK IS TIMER B2
LOWER NIBBLE CLOCK IS PERCLK
LOWER NIBBLE CLOCK IS TIMER A1
LOWER NIBBLE CLOCK IS TIMER B1
LOWER NIBBLE CLOCK IS TIMER B2

PORT x ALTERNATE LOW REGISTERS
PCALR (0x52) PEALR (0x72)
PDALR (0x62)
SELECT BIT 3 ALTERNATE OUTPUT
SELECT BIT 2 ALTERNATE OUTPUT
SELECT BIT 1 ALTERNATE OUTPUT
SELECT BIT 0 ALTERNATE OUTPUT

PORT x ALTERNATE HIGH REGISTERS
PCAHR (0x53) PEAHR (0x73)
PDAHR (0x63)
SELECT BIT 7 ALTERNATE OUTPUT
SELECT BIT 6 ALTERNATE OUTPUT
SELECT BIT 5 ALTERNATE OUTPUT
SELECT BIT 4 ALTERNATE OUTPUT

PORT x BIT y REGISTERS
PDB0R (0x78) PEB0R (0x88)
PDB1R (0x79) PEB1R (0x89)
PDB2R (0x7A) PEB2R (0x8A)
PDB3R (0x7B) PEB3R (0x8B)
PDB4R (0x7C) PEB4R (0x8C)
PDB5R (0x7D) PEB5R (0x8D)
PDB6R (0x7E) PEB6R (0x8E)
PDB7R (0x7F) PEB7R (0x8F)
A WRITE TO THE CORRESPONDING BIT CHANGES THAT BIT

PARALLEL PORT A*

PIN	I/O	SLAVE	AUX I/O
PA7	PARALLEL I/O	SLAVE DATA	AUX I/O DATA
PA6			
PA5			
PA4			
PA3			
PA2			
PA1			
PA0			

*SELECTION VIA SPCR

PARALLEL PORT B*

PIN	SLAVE	SERIAL	AUX I/O
PB7	/ATTN		IA5
PB6	/SCS		IA4
PB5	SA1		IA3
PB4	SA0		IA2
PB3	/SRD		IA1
PB2	/SWR		IA0
PB1		SCLKA	IA7
PB0		SCLKB	IA6

*SELECTION VIA SPCR, SACR, SBCR

ALTERNATE INPUT FUNCTIONS: PORTS C, D, E

PARALLEL PORT C

PIN	SERIAL ABCD	SERIAL EF	INPUT CAPT
PC7	RXA	RXE	YES
PC6			
PC5	RXB	RCLKE	YES
PC4		TCLKE	
PC3	RXC	RXF	YES
PC2			
PC1	RXD	RCLKF	YES
PC0		TCLKF	

PARALLEL PORT D

PIN	SERIAL ABCD	SERIAL EF	INPUT CAPT	DMA & INT	QUAD DEC	AUX I/O
PD7	RXA	RXE	YES			16-BIT DATA
PD6						
PD5	RXB	RCLKE	YES			
PD4		TCLKE				
PD3	RXC	RXF	YES	DREQ1	QRD2A	
PD2	SCLKC			DREQ0	QRD2B	
PD1	RXD	RCLKF	YES	INT1	QRD1A	
PD0	SCLKD	TCLKF		INT0	RQD1B	

PARALLEL PORT E

PIN	SERIAL ABCD	SERIAL EF	INPUT CAPT	DMA & INT	QUAD DEC	NET	SLAVE	I/O HANDSH
PE7	RXA	RXE	YES	DREQ1	QRD2A		/SCS	YES
PE6				DREQ0	QRD2B	ECLK		YES
PE5	RXB	RCLKE	YES	INT1	QRD1A			YES
PE4		TCLKE		INT0	QRD1B			YES
PE3	RXC	RXF	YES	DREQ1	QRD2A			YES
PE2	SCLKC			DREQ0	QRD2B			YES
PE1	RXD	RCLKF	YES	INT1	QRD1A			YES
PE0	SCLKD	TCLKF		INT0	QRD1B			YES

ALTERNATE OUTPUT FUNCTIONS: PORTS C, D, E

PARALLEL PORT C

PIN	ALT0	ALT1	ALT2	ALT3
PC7	TXA	I7	PWM3	SCLKC
PC6	TXA	I6	PWM2	TXE
PC5	TXB	I5	PWM1	RCLKE
PC4	TXB	I4	PWM0	TCLKE
PC3	TXC	I3	TMRC3	SCLKD
PC2	TXC	I2	TMRC2	TXF
PC1	TXD	I1	TMRC1	RCLKF
PC0	TXD	I0	TMRC0	TCLKF

PARALLEL PORT D

PIN	ALT0	ALT1	ALT2	ALT3
PD7	IA7	I7	PWM3	SCLKC
PD6	TXA	IA6	PWM2	TXE
PD5	IA6	I5	PWM1	RCLKE
PD4	TXB	I4	PWM0	TCLKE
PD3	IA7	I3	TMRC3	SCLKD
PD2	SCLKC	I2	TMRC2	TXF
PD1	IA6	I1	TMRC1	RCLKF
PD0	SCLKD	I0	TMRC0	TCLKF

PARALLEL PORT E

PIN	ALT0	ALT1	ALT2	ALT3
PE7	I7	/ACT	PWM3	SCLKC
PE6	I6		PWM2	TXE
PE5	I5	/LINK	PWM1	RCLKE
PE4	I4	/A0	PWM0	TCLKE
PE3	I3	A23	TMRC3	SCLKD
PE2	I2	A22	TMRC2	TXF
PE1	I1	A21	TMRC1	ACLKF
PE0	I0	A20	TMRC0	TCLKF

Serial Ports

SERIAL PORT x DATA REGISTER (SxDR)
SADR (0xC0) SBDR (0xD0)
SCDR (0xE0) SDDR (0xF0)
SEDR (0xC8) SFDR (0xD8)
RD = RETURNS CONTENTS OF RCV BUFFER
WR = LOADS XMIT BUF WITH BYTE BYTE FOR TRANSMISSION

SERIAL PORT x ADDRESS REGISTER**
SAAR (0xC1) SBAR (0xD1)
SCAR (0xE1) SDAR (0xF1)
SEAR (0xC9) SFAR (0xD9)
RD = RETURNS CONTENTS OF RCV BUFFER
W R = LOADS XMIT BUF WITH ADDRESS BYTE FOR TRANSMISSION (9TH BIT=0)

SERIAL PORT x LONG STOP REGISTER (SxLR)
SALR (0xC2) SBLR (0xD2)
SCLR (0xE2) SDLR (0xF2)
SELR (0xCA) SFLR (0xDA)
RD = RETURNS CONTENTS OF RCV BUFFER
WR = LOAD ADDRESS BYTE. MARK ADDRESS BIT = 1. HDLC MODE – WRITE LAST BYTE OF FRAME – ENABLE CLOSE FLAG TRANSMISSION

SERIAL PORT x STATUS REGISTER (SxSR)**
SASR (0xC3) SCSR (0xE3) SESR (0xCB)
SBSR (0xD3) SDSR (0xF3) SFSR (0xDB)

RCV DATA REG. — 0 = EMPTY; 1 = FULL. REQUESTS INTERRUPT. CLEARED WHEN RCV BUF READ
RCV BUF — 0 = BYTE IN RCV BUF IS DATA; 1 = BYTE IN RCV BUF IS ADDRESS
RCV BUF — 0 = RCV BUF NOT OVERRUN; 1 = RCV BUF OVERRUN. CLEARED WHEN RVC BUF READ
RCV PARITY — 0 = BYTE IN RCV BUF HAS PARITY OK; 1 = BYTE IN RCV BUF HAS PARITY ERROR
XMIT DATA REG — 0 = EMPTY. REQUESTS INTERRUPT; 1 = FULL***
XMIT — 0 = IDLE. REQUESTS INTERRUPT; 1 = SENDING BYTE
ALWAYS 0

SERIAL PORT x EXTENDED REGISTER
SAER (0xC5) SBER (0xD5) SCER (0xE5) SDER (0xF5) SEER (0xCD) SFER (0xDD)

ASYNC MODE (A,B,C,D,E,F)
RESERVED
000 = DISABLE PARITY
100 = ENABLE EVEN PARITY
101 = ENABLE ODD PARITY
110 = ENABLE SPACE PARITY
111 = ENABLE MARK PARITY
0 = NORMAL CODING
1 = R21 (3/16 IrDA)
0 = NORMAL BREAK
1 = FAST BREAK
0 = ASYNC CLK = 16x
1 = ASYNC CLK = 8x
0 = CHAR ASSY DURING BREAK
1 = NO CHAR ASSY DURING BREAK

CLOCKED MODE (A,B,C,D)
0 = NORMAL CLOCK
1 = TIMED CLOCK
0 = TIMED BY TIMER B1
1 = TIMED BY TIMER B2
00 = NORMAL CLK, INACTIVE HIGH, INT OR EXT CLK
01 = NORMAL CLK, INACTIVE LOW, INT CLK
10 = INVERTED CLK, INACTIVE LOW, INT OR EXT CLK
11 = INVERTED CLK, INACTIVE HIGH, INT CLK
0 = NORMAL DATA BIT ORDER
1 = REVERSE DATA BIT ORDER
0 = CLOCK INPUT FROM PARALLEL PORT D (SCER, SDER)
1 = CLOCK INPUT FROM PARALLEL PORT E (SCER, SDER)
TERMINATE XMIT
TERMINATE RCV

HDLC MODE (E,F)
000 = NRZ CODING
010 = NRZI CODING
100 = BI-PHASE LEVEL CODING (MANCHESTER)
110 = BI-PHASE SPACE CODING (FM0)
111 = BI-PHASE MARK CODING (FM1)
0 = NORMAL CODING
1 = IrDA (1/4b RZI CODING (W/NRZ & INT CLK)
0 = IDLE LINE COND. = FLAG
1 = IDLE LINE COND. = ONE
0 = XMIT FLAG ON UNDERRUN
1 = XMIT ABORT ON UNDERRUN
0 = SEPARATE EXTERNAL RCV/XMIT CLOCKS
1 = COMBINED EXTERNAL RCV/XMIT CLOCKS (XMIT PIN)

SERIAL PORT x CONTROL REGISTER (SxCR)
SACR (0xC4) SBCR (0xD4) SECR (0xCC) SFCR (0xDC)
SCCR (0xE4) SDCR (0xF4)

(A–D)
00 = NO OPERATION. IGNORED IN ASYNCH MODE
01 = CLOCKED MODE: START BYTE RCV OPERATION
10 = CLOCKED MODE: START BYTE XMIT OPERATION
11 = CLOCKED MODE: START RCV & XMIT
00 = PARALLEL PORT C USED FOR INPUT
01 = PARALLEL PORT D USED FOR INPUT
10 = PARALLEL PORT E USED FOR INPUT
11 = DISBALE RCV INPUT
00 = ASYNCH MODE: 8 BITS PER CHAR.
01 = ASYNCH MODE: 7 BITS PER CHAR.
10 = CLOCKED MODE: EXTERNAL CLOCK (INPUT)
11 = CLOCKED MODE: INTERNAL CLOCK (OUTPUT)
INTERRUPT — 00 = DISABLED; 01 = PRIORITY 1; 10 = PRIORITY 2; 11 = PRIORITY 3

(E, F)
00 = NO OPERATION (IGNORED IN ASYNCH MODE)
01 = HDLC MODE: FORCE FLAG SEARCH MODE
10 = NO OPERATION
11 = HDLC MODE: TRANSMIT ABORT PATTERN
00 = PARALLEL PORT C USED FOR INPUT
01 = PARALLEL PORT D USED FOR INPUT
10 = PARALLEL PORT E USED FOR INPUT
11 = DISABLE RCV INPUT
00 = ASYNCH MODE: 8 BITS PER CHAR.
01 = ASYNCH MODE: 7 BITS PER CHAR.
10 = HDLC MODE: EXTERNAL CLOCK (INPUT)
11 = HDLC MODE: INTERNAL CLOCK (OUTPUT)
INTERRUPT — 00 = DISABLED; 01 = PRIORITY 1; 10 = PRIORITY 2; 11 = PRIORITY 3

SERIAL PORT x DIVIDER HIGH REGISTER
SADHR (0xC7) SBDHR (0xD7)
SCDHR (0xE7) SDDHR (0xF7)
SEDHR (0xCF) SFDHR (0xDF)

SERIAL PORT x DIVIDER LOW REGISTER
SADLR (0xC6) SBDLR (0xD6)
SCDLR (0xE6) SDDLR (0xF6)
SEDLR (0xCE) SFDLR (0xDE)

ENABLE DEDICATED DIVIDER — 15-BIT DIVIDER VALUE

ASYNCH ONLY (REFER TO MANUAL FOR CLOCKED SERIAL & HDLC) * TX INTERRUPTS ARE CLEARED WITH A WRITE TO THE SxSR

Write Protect

WRITE PROTECT CONTROL REGISTER
WPCR (0x440)
0 0 0 0 0 0 0
0 = ENABLE WRITE PROTECTION IN USER MODE ONLY
1 = ENABLE WRITE PROTECTION IN ALL MODES

WRITE PROTECT LOW/HIGH REGISTERS
WP0R (0x460) – WP31R (0x47F)
0 = DISABLE WRITE PROTECT FOR 64 KB BLOCK
1 = ENABLE WRITE PROTECT FOR 64 KB BLOCK

WRITE PROTECT SEGMENT REGISTERS
WPSAR (0x480) WPSBR (0x484)
WHEN THESE MATCH PHYSICAL ADDRESS [23:16], SUBDIVIDE WRITE PROTECT FOR THAT 64KB BLOCK INTO 4 KB BLOCKS

WRITE PROTECT SEGMENT LOW/HIGH REGISTERS
WPSALR (0x481) WPSAHR (0x482)
WPSBLR (0x485) WPSBHR (0x486)
0 = DISABLE WRITE PROTECT FOR 4 KB BLOCK
1 = ENABLE WRITE PROTECT FOR 4 KB BLOCK

Real-Time Clock

REAL-TIME CLOCK x REGISTER
RTC0R (0x02) R/W
RTC1R (0x03) RD
RTC2R (0x04) RD
RTC3R (0x05) RD
RTC4R (0x06) RD
RTC5R (0x07) RD
RD = CURRENT VALUE OF 48-BIT RTC HOLDING REGISTER IS RETURNED
W = A WRITE TO RTC0R TRANSFERS CURRENT COUNT OF RTC TO HOLDING REGISTER

REAL-TIME CLOCK CONTROL REGISTER
RTCCR (0x01)
RTC5B RTC4B RTC3B RTC2B RTC1B RTC0B
01 = THIS BIT COMBINATION MUST BE USED WITH EVERY BYTE INCREMENT WRITE
0 = NO EFFECT ON RTC COUNTER
1 = INCREMENT CORRESPONDING BYTE OF RTC (RTCxB)

RTCCR (SHORTCUTS)
0x00 = NO EFFECT ON RTC COUNTER DISABLE BYTE INCREMENT CANCEL RTC COMMAND
0x40 = ARM RTC FOR RESET OR BYTE INCREMENT. THIS COMMAND MUST BE WRITTEN PRIOR TO RTC RESET OR FIRST BYTE RESET
0x80 = RESET ALL SIX BYTES OF RTC TO 0x00. RESET MUST BE PRECEDED BY WRITING 0x40 TO ARM RESET FUNCTION
0xC0 = RESET ALL SIX BYTES IN RTC COUNTER TO 0x00 AND REMAIN IN BYTE INCREMENT MODE

Stack Limit Protection

STACK LIMIT CONTROL REGISTER
STKCR (0x444)
0 0 0 0 0 0 0
0 = DISABLE STACK LIMIT CHECKING
1 = ENABLE STACK LIMIT CHECKING

STACK LOW LIMIT REGISTER
STKLLR (0x445)
SET LOWER LIMIT FOR STACK LIMIT CHECKING
IF STACK ACCESS ATTEMPTED BELOW {STKLLR, 0x10} INTERRUPT OCCURS

STACK HIGH LIMIT REGISTER
STKHLR (0x446)
SET UPPER LIMIT FOR STACK LIMIT CHECKING
IF STACK ACCESS ATTEMPTED ABOVE {STKHLR, 0xEF} INTERRUPT OCCURS

System/User Mode

ENABLE DUAL-MODE REGISTER
EDMR (0x420)
0 0 0 0 0
0 = DISABLE SYSTEM/USER MODE
1 = ENABLE SYSTEM/USER MODE
00 = RABBIT 3000 INSTRUCTION SET
11 = RABBIT 4000 INSTRUCTION SET

PERIPHERAL USER ENABLE REGISTERS

RTUER (0x300)	PWUER (0x388)
SPUER (0x320)	QDUER (0x390)
PAUER (0x330)	TAUER (0x3A0)
PBUER (0x340)	TBUER (0x3B0)
PCUER (0x350)	SAUER (0x3C0)
PDUER (0x360)	SBUER (0x3D0)
PEUER (0x370)	SCUER (0x3E0)
PFUER (0x338)	SDUER (0x3F0)
PGUER (0x348)	SEUER (0x3C8)
ICUER (0x358)	SFUER (0x3D8)
TCUER (0x3F8)	

0 0 0 0 0 0 0 0
0 = DISABLE USER MODE ACCESS TO PERIPHERAL
1 = ENABLE USER MODE ACCESS TO PERIPHERAL

I/O BANK USER ENABLE REGISTER
IBUER (0x380)
0 = DISABLE USER MODE ACCESS TO I/O BANK
1 = ENABLE USER MODE ACCESS TO I/O BANK

EXTERNAL INTERRUPT USER ENABLE REGISTER
IUER (0x398)
0 0 0 0 0 0
0 = DISABLE USER MODE ACCESS TO EXT INT 1
1 = ENABLE USER MODE ACCESS TO EXT INT 1
0 = DISABLE USER MODE ACCESS TO EXT INT 0
1 = ENABLE USER MODE ACCESS TO EXT INT 0

Quadrature Decoder

(USES TIMER A10)

QUAD DECODE CONTROL REGISTER
QDCR (0x91)
00 = QD2 INPUT DISABLED
01 = QD2 INPUT FROM PD3 & PD2
10 = QD2 INPUT FROM PE3 & PE2
11 = QD2 INPUT FROM PE7 & PE6
0 = 8-BIT COUNTER
1 = 10-BIT COUNTER
00 = QD1 INPUT DISABLED
01 = QD1 INPUT FROM PD1 & PD0
10 = QD1 INPUT FROM PE1 & PE0
11 = QD1 INPUT FROM PE5 & PE4
00 = QD INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

QUAD DECODE CONTROL/STATUS REGISTER
QDCSR (0x90)
1 = QD2 = INCREMENTED FROM MAX → 0x00
1 = QD2 = DECREMENTED FROM 0x00 → MAX
ALWAYS ZERO
RESET QD2
1 = QD1 = INCREMENTED FROM MAX → 0x00
1 = QD1 = DECREMENTED FROM 0x00 → MAX
ALWAYS ZERO
RESET QD1

QUAD DECODE COUNT REGISTER
QDC1R (0x94) QDC2R (0x96)
BITS 0-7 OF QD COUNT

QUAD DECODE HIGH COUNT REGISTER
QDC1HR (0x95) QDC2HR (0x97)
0 0 0 0 0 0
BITS 8-9 OF QD COUNT

Tamper-Protect RAM

TAMPER -PROTECT BYTE X

VRAM00 (0x0600)	VRAM08 (0x0608)	VRAM16 (0x0610)	VRAM24 (0x0618)
VRAM01 (0x0601)	VRAM09 (0x0609)	VRAM17 (0x0611)	VRAM25 (0x0619)
VRAM02 (0x0602)	VRAM10 (0x060A)	VRAM18 (0x0612)	VRAM26 (0x061A)
VRAM03 (0x0603)	VRAM11 (0x060B)	VRAM19 (0x0613)	VRAM27 (0x061B)
VRAM04 (0x0604)	VRAM12 (0x060C)	VRAM20 (0x0614)	VRAM28 (0x061C)
VRAM05 (0x0605)	VRAM13 (0x060D)	VRAM21 (0x0615)	VRAM29 (0x061D)
VRAM06 (0x0606)	VRAM14 (0x060E)	VRAM22 (0x0616)	VRAM30 (0x061E)
VRAM07 (0x0607)	VRAM15 (0x060F)	VRAM23 (0x0617)	VRAM31 (0x061F)

ACCESS TAMPER-PROTECTED BYTE

External I/O

I/O ADDRESS A15 A14 A13	I/O BANK	CONTROL REGISTER		PORT SIGNAL
1 1 1		IB7CR	(0x87)	I7
1 1 0		IB6CR	(0x86)	I6
1 0 1		IB5CR	(0x85)	I5
1 0 0		IB4CR	(0x84)	I4
0 1 1		IB3CR	(0x83)	I3
0 1 0		IB2CR	(0x82)	I2
0 0 1		IB1CR	(0x81)	I1
0 0 0		IB0CR	(0x80)	I0

I/O BANK x CONTROL REGISTER (IBxCR)
WAITS STATES
00 = 15 WS
01 = 7 WS
10 = 3 WS
11 = 1 WS
I/O STROBE FUNCTIONS (IX)
00 = I/O /CS
01 = I/O /RD STROBE
10 = I/O /WR STROBE
11 = I/O DATA (/RD OR /WR) STROBE
1 = WRITES ALLOWED
0 = WRITES NOT ALLOWED
1 = ACTIVE HIGH STROBE
0 = ACTIVE LOW STROBE
0 = NORMAL I/O TRANSACTION TIMING
1 = SHORTEN READ/WRITE STROBES
0 = USE I/O BUS IF ENABLED
1 = ALWAYS USE MEMORY DATA BUS

I/O HANDSHAKE TIMEOUT REGISTER
IHTR (0x002A)
0
HANDSHAKE TIMEOUT COUNTER IN UNITS OF 32 CLOCKS
0 = NO TIMEOUT OCCURRED
1 = TIMEOUT OCCURRED

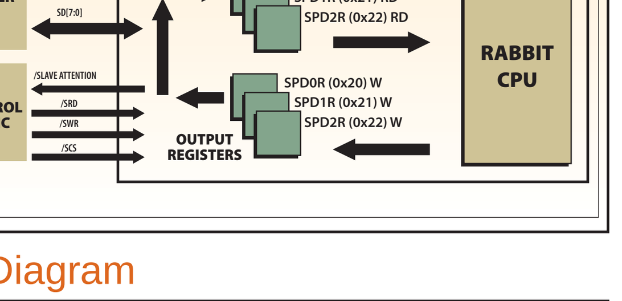
I/O HANDSHAKE CONTROL REGISTER
IHCR (0x0028)
0 0 0 0 0
0 = I/O HANDSHAKE ACTIVE LOW
1 = I/O HANDSHAKE ACTIVE HIGH
000 = HANDSHAKE WITH PE0
001 = HANDSHAKE WITH PE1
010 = HANDSHAKE WITH PE2
011 = HANDSHAKE WITH PE3
100 = HANDSHAKE WITH PE4
101 = HANDSHAKE WITH PE5
110 = HANDSHAKE WITH PE6
111 = HANDSHAKE WITH PE7

I/O HANDSHAKE SELECT REGISTER
IHSR (0x0029)
0 = DISABLE HANDSHAKE FOR I/O BANK
1 = ENABLE HANDSHAKE FOR I/O BANK

Slave Port

SLAVE PORT CONTROL REGISTER
SPCR (0x24)
0 = PROGRAM FETCH AS A FUNCTION OF SMODE PINS
1 = IGNORE SMODE PINS
(RD) = REPORT STATE OF SMODE PINS
(WR) = IGNORED FOR WRITE
000 = DISABLE SLAVE PORT. PORT A IS BYTE WIDE INPUT
001 = DISABLE SLAVE PORT. PORT A IS BYTE WIDE OUTPUT
010 = ENABLE SLAVE PORT. /SCS ON PE7
011 = ENABLE AUX I/O BUS. ADDRESS ON PB[7:2]
110 = ENABLE SLAVE PORT. /SCS ON PB6
111 = ENABLE AUX I/O BUS. ADDRESS ON PB[7:0]
00 = SLAVE PORT INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

SLAVE PORT STATUS REGISTER
SPSR (0x23)
0 = PROCESSOR WROTE TO SPSR
1 = MASTER WROTE TO SPD0R
READ CORRESPONDING PORT STATUS
0 = EMPTY
1 = FULL
0 = MASTER WROTE TO STATUS REG
1 = PROCESSOR WROTE TO SPD0R
WRITE CORRESPONDING PORT STATUS
0 = EMPTY
1 = FULL



Input Capture

(USES TIMER A8)

INPUT CAPTURE CONTROL/STATUS REGISTER
ICCSR (0x56)

READ	WRITE
IC2 START CONDITION OCCURRED	ENABLE IC2 START INT.
IC2 STOP CONDITION OCCURRED	ENABLE IC2 STOP INT.
IC1 START CONDITION OCCURRED	ENABLE IC1 START INT.
IC1 STOP CONDITION OCCURRED	ENABLE IC1 STOP INT.
IC2 ROLLED OVER	RESET IC2 COUNTER & ROLLOVER LATCH
IC1 ROLLED OVER	RESET IC1 COUNTER & ROLLOVER LATCH
RESERVED MUST = 0	

CLEARED WHEN READ

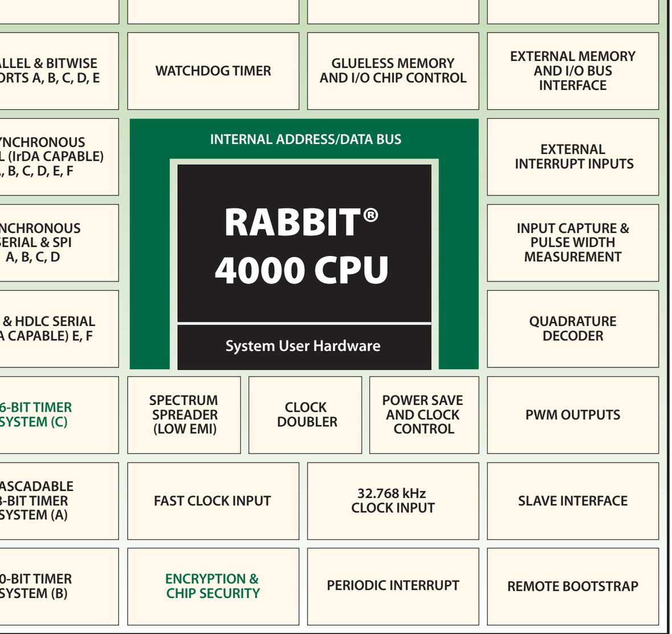
INPUT CAPTURE CONTROL REGISTER
ICCR (0x57)
0 = IC2 NORMAL OPERATION
1 = IC2 COUNTER OPERATION
0 = IC1 NORMAL OPERATION
1 = IC1 COUNTER OPERATION
RESERVED MUST = 0
00 = INPUT CAPTURE INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

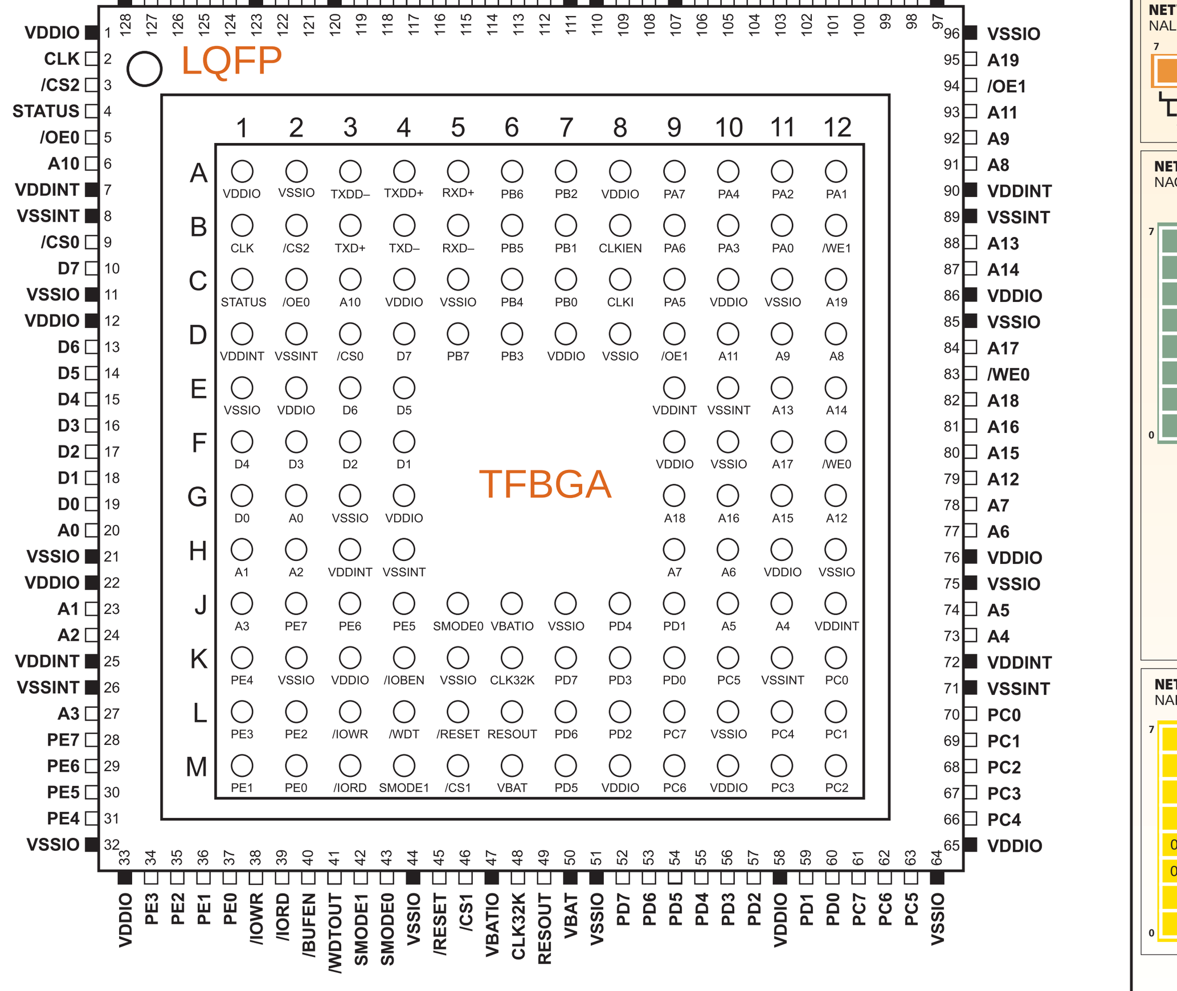
INPUT CAPTURE SOURCE x REGISTERS
ICS1R (0x59) — ICS2R (0x5D)
USE: 00 = PORT C; 01 = PORT D; 10 = PORT E; 11 = RESERVED
00 = BIT 1; 01 = BIT 3; 10 = BIT 5; 11 = BIT 7 — AS START CONDITIONS INPUT
USE: 00 = PORT C; 01 = PORT D; 10 = PORT E; 11 = RESERVED
00 = BIT 1; 01 = BIT 3; 10 = BIT 5; 11 = BIT 7 — AS STOP CONDITIONS INPUT

INPUT CAPTURE TRIGGER x REGISTERS
ICT1R (0x58) — ICT2R (0x5C)
00 = COUNTER DISABLED
01 = COUNT FROM START TO STOP
10 = COUNT CONTINUOUSLY
11 = COUNT UNTIL STOP
00 = DISABLE LATCH
01 = LATCH COUNTER ON STOP
10 = LATCH COUNTER ON START
11 = LATCH COUNTER ON START & STOP
00 = IGNORE START INPUT
01 = START AT START INPUT RISING EDGE
10 = START AT START INPUT FALLING EDGE
11 = START AT START INPUT EITHER EDGE
00 = IGNORE STOP INPUT
01 = STOP AT STOP INPUT RISING EDGE
10 = STOP AT STOP INPUT FALLING EDGE
11 = STOP AT STOP INPUT EITHER EDGE

INPUT CAPTURE COUNTER REGISTER
MSB — ICM1R (0x5B) ICM2R (0x5F)
READ MSB (RE-OPENS LATCH)
LSB — ICL1R (0x5A) ICL2R (0x5E)
READ LSB (LATCHES MSB)

Block Diagram





Network Port A

NETWORK DATA REGISTER
NADR (0x0200) (DMA ACCESS ONLY)
RD = RETURNS CONTENT OF RECEIVE BUFFER
WR = LOAD TRANSMIT BUFFER

NETWORK LAST DATA REGISTER
NALDR (0x0201) (DMA ACCESS ONLY)
RD = RETURNS CONTENT OF RECEIVE BUFFER
WR = LOAD TRANSMIT BUFFER

NETWORK TRANSMIT STATUS REGISTER
NATSR (0x0202)
0000=TRANSMITTER DISABLED
0xx1=TRANSMIT ABORTED; FIFO UNDERRUN
0x1x=TRASMIT ABORTED; 16 COLLISIONS
01xx=TRANSMITTER IS DEFERRING TRANSMISSION
1000=TRANSMITTED WITHOUT ERROR
0=NO COLLISIONS DETECTED
1=AT LEAST 1 COLLISION DETECTED
0=NO LATE COLLISIONS DETECTED
1=LATE COLLISION DETECTED

NETWORK RESET REGISTER
NARR (0x0206)
0 = NO OPERATION
1 = RESET RECEIVER
0 = NO OPERATION
1 = RESET TRANSMITTER
0 = NO OPERATION
1 = PURGE RECEIVE FIFO
0 = NO OPERATION
1 = PURGE TRANSMIT FIFO

NETWORK CONTROL REGISTER
NACR (0x0207)
00 = DISABLE CLOCK
01 = CLOCK FROM PE6
10 = CLOCK FROM SYSTEM CLOCK
11 = CLOCK FROM SYSTEM CLOCK/2
0 = NORMAL OPERATION
1 = RESTART AUTO-NEGOTIATION
0 = DISABLE AUTO-NEGOTIATION
1 = ENABLE DAUTO-NEGOTIATION
0 = FORCE HALF-DUPLEXING
1 = ENABLE FULL-DUPLEXING

NETWORK CONTROL/STATUS REGISTER
NACSR (0x0204)
WR 0 = DISABLE INTERRUPT
WR 1 = ENABLE INTERRUPT
RD 0 = NO FRAME RECEIVED
RD 1 = FRAME RECEIVED ERROR-FREE
WR 0 = DISABLE INTERRUPT
WR 1 = ENABLE INTERRUPT
RD 0 = NO FRAME RECEIVED
RD 1 = FRAME RECEIVED WITH ERRORS
WR 0 = DISABLE INTERRUPT
WR 1 = ENABLE INTERRUPT
RD 0 = TRANSMISSION NOT COMPLETE
RD 1 = TRANSMISSION ERROR-FREE
WR 0 = DISABLE INTERRUPT
WR 1 = ENABLE INTERRUPT
RD 0 = TRANSMISSION ERROR-FREE
RD 1 = TRANSMISSION ABORTED WITH ERROR
WR 0 = DISABLE INTERRUPT
WR 1 = ENABLE INTERRUPT
RD 0 = NO ERROR COUNTERS NOT OVERFLOWS
RD 1= 1 OR MORE ERROR COUNTERS OVERFLOWED
WR 0 = DISABLE INTERRUPT
WR 1 = ENABLE INTERRUPT
RD 0 = NO LINK FAILURE OR JABBER
RD 1 = STATUS CHANGE OR JABBER DETECTED
00 = INTERRUPT DISABLED
01 = PRIORITY 1 INTERRUPT
10 = PRIORITY 2 INTERRUPT
11 = PRIORITY 3 INTERRUPT

NETWORK TRANSMIT CONTROL REGISTER
NATCR (0x020A)
0 = DISABLE TRANSMITTER
1 = ENABLED TRANSMITTER
0 = DMA REQUEST WHEN FIFO IS HALF EMPTY
1 = DMA REQUEST WHEN FIFO IS ONE-FOURTH EMPTY

NETWORK PIN CONTROL REGISTER
NAPCR (0x0208)
IF NACR BITS 7, 6 NON-ZERO
000 = RxD+ SIGNAL RxD- QUALIFIER
010 = RxD+ SIGNAL RxD- INVERTED QUALIFIER
100 = RxD+ SIGNAL
110 = RxD+ INVERTED SIGNAL
001 = RxD IS ZERO CROSS DETECTOR RxD- 300 mV OFFSET DETECTOR
011,101, 111 = TEST MODE ONLY
READ ONLY PIN STATE
IF NACR BITS 7, 6 ZERO
IGNORED
WR = DRIVE TXDD+ WITH VALUE
RD = STATE OF TXDD
WR = DRIVE TXD+ WITH VALUE
RD = STATE OF TXD+
WR = DRIVE TXDD- WITH VALUE
RD = STATE OF TXDD
WR = DRIVE TXD- WITH VALUE
RD = STATE OF TXD-
WR = IGNORED
RD = STATE OF RXD+
WR = IGNORED
RD = STATE OF RXD-

NETWORK RECEIVE CONTROL REGISTER
NARCR (0x020B)
0=DISABLE RECEIVER
1=ENABLE RECEIVER
0=DMA REQUEST WHEN FIFO IS HALF FULL
1=DMA REQUEST WHEN FIFO IS ONE-FOURTH FULL
0=NORMAL RECEIVER OPERATION
1=PLACE RECEIVER IN MONITOR MODE
0=DISCARD FRAMES LESS THAN 64 BYTES
1=ACCEPT FRAMES AS SHORT AS 8 BYTES
0=DISCARD FRAMES WITH ERRORS
1=ACCPET FRAMES WITH ERRORS
0=IGNORE BROADCAST FRAMES
1=ACCEPT BROADCAST FRAMES
0=IGNORE MULTICASTED FRAMES
1=ACCEPT MULTICASTED FRAMES
0=IGNORE FRAMES WITH PHYSICAL ADDRESS MISMATCH
1=ACCEPT FRAMES WITH ANY PHYSICAL ADDRESS

NETWORK RECEIVE STATUS REGISTER
NARSR (0x0203)
0000 = RECEIVER DISABLED
0xx1 = FRAME DISCARDED; FIFO UNDERRUN
0x1x = FRAME DISCARDED; ALIGNMENT ERROR
01xx = FRAM DISCARDED; CRC ERROR
1000 = FRAME RECEIVED WITHOUT ERROR
00 = FRAME HAD PHYSICAL ADDRESS MATCH
01 = FRAME DID NOT HAVE PHYSICAL ADDRESS MATCH
10 = FRAME HAD MULTICAST ADDRESS MATCH
11 = FRAME HAD BROADCAST ADDRESS MATCH

NETWORK PHYS. ADDR x REGISTER
NAPA0R (0x0210) NAPA1R (0x0211)
NAPA2R (0x0212) NAPA3R (0x0213)
NAPA4R (0x0214) NAPA5R (0x0215)
BYTE OF PHYISCAL ADDRESS FOR RECEIVE ADDRESS FILTERING

NETWORK MULTI. FILTER x REGISTER
NAMF0R (0x0218) NAMF1R (0x0219)
NAMF2R (0x021A) NAMF3R (0x021B)
NAMF4R (0x021C) NAMF5R (0x021D)
NAMF6R (0x021E) NAMF7R (0x021F)
BITS OF MULTICAST FILTER

NETWORK STATUS REGISTER
NASR (0x0205)
0 = HALF DUPLEX
1 = FULL DUPLEX
0 = AUTO-NEGOTIATOIN NOT COMPLETE
1 = AUTO-NEGOTIATION COMPLETE
0 = LINK IS DOWN
1 = LINK IS UP
0 = NO JABBER DETECTED
1 = JABBER DETECTED

NETWORK MULTICAST HASH REGISTER
NAMHR (0x0220)
HASH VALUE

NETWORK COLLISION DETECT REGISTER
NACDR (0x0221)
VALUE OF COLLISION DETECT COUNTER

NETWORK ALIGNMENT ERROR REGISTER
NAAER (0x0222)
VALUE OF ALIGNMENT ERROR COUNTER

NETWORK CRC ERROR REGISTER
NACER (0x0223)
VALUE OF CRC ERROR COUNTER

NETWORK CHECKSUM x REGISTER
NAC1R (0x0225) NAC0R (0x0224)
NAC1R NAC0R — CHECKSUM

NETWORK MISSED FRAME REGISTER
NAMFR (0x0226)
VALUE OF MISSED FRAM COUNTER

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