# *Digi NS9210/NS9215 FIM SPI Port Implementation*

Supplemental Reference

90002114_A
11/19/2010

# Using this Guide

## Digi Information

### *Document Updates*

Please always check the product specific section on the Digi support website at www.digiembedded.com/support for the most current revision of this document.

### *Contact Information*

For more information about your Digi products, or for customer service and technical support, contact Digi International.

| To contact Digi International by | Use |
|---|---|
| Mail | Digi International<br>1101 Bren Road East<br>Minnetonka, MN 55343<br>U.S.A |
| World Wide Web | http://www.digiembedded.com/support/ |
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### *For use in conjunction with:*

NS9210 Hardware Reference
Part number/ version: 90000846_H
Release date: November 2010

NS9215 Hardware Reference
Part number/version: 90000847_J
Release date: November 2010

NS9210/NS9215 Errata
Part number/version: 90002007_C
Release date: November 2010

# FIM SPI Implementation Overview

## FIM-based SPI Port

The FIM-based SPI port implementation for the Digi NS9210/NS9215 provides support for mode 0, 1, 2, and 3 with a maximum data rate of 21 Mbps on a system with a 75MHz AHB clock speed. Only master mode is supported. Slave mode is not supported. The parallel operation of SPI ports in both FIMs is supported.

Software access to the FIM-based SPI port is abstracted as part of the standard SPI driver API. Please also refer to the API reference of your software platform for general information.

The I/O setup for the FIM SPI ports is user-configurable, including the use of standard GPIO pins for the CS signal, as implemented in the standard driver.

The tables below outline the default I/O configuration.

**Table 1: Port 4 (FIM0)**

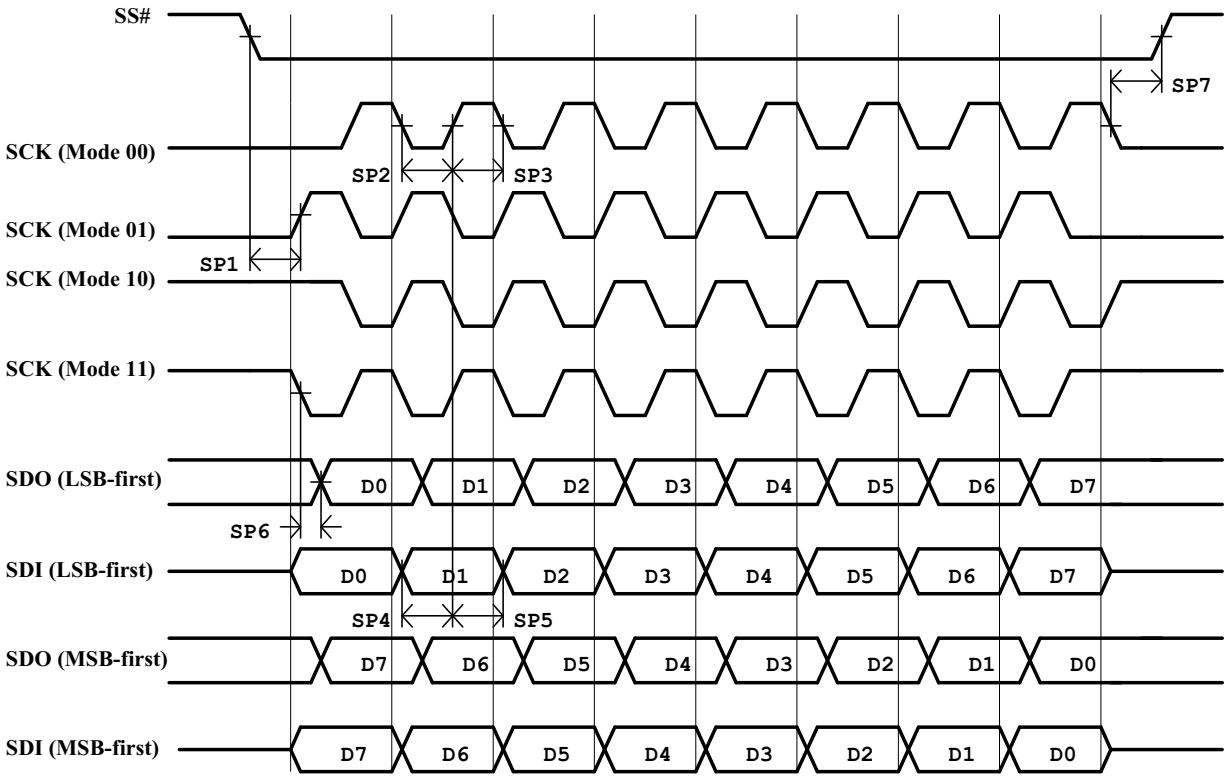
| Signal | FIM Function | NS9210 Pin | NS9215 Pin | SPI Function |
|---|---|---|---|---|
| GPIO [0] | PIC_0_GEN_IO[0] | G12 | K15 | SPI In (SDI) |
| GPIO [1] | PIC_0_GEN_IO[1] | H13 | K17 | SPI Clock (SCK) |
| GPIO [2] | PIC_0_GEN_IO[2] | H12 | J17 | SPI Out (SDO) |
| GPIO [3] | PIC_0_GEN_IO[3] | H15 | J16 | SPI Enable (SS#) |

**Table 2: Port 5 (FIM1)**

| Signal | FIM Function | NS9210 Pin | NS9215 Pin | SPI Function |
|---|---|---|---|---|
| GPIO [26] | PIC_0_GEN_IO[0] | F2 | F4 | SPI In (SDI) |
| GPIO [27] | PIC_0_GEN_IO[1] | F4 | F3 | SPI Clock (SCK) |
| GPIO [28] | PIC_0_GEN_IO[2] | G2 | G5 | SPI Out (SDO) |
| GPIO [29] | PIC_0_GEN_IO[3] | G3 | G4 | SPI Enable (SS#) |

The FIM based SPI port implementation is currently available for NET+OS and Digi Embedded Linux. Please contact Digi technical support for additional information.

## NS9210 FIM/SPI Timing (Fast mode)




| Parameter | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| SP1 | Chip select active to CLK (tx edge) | 16 | | Tc(FIM) | 1, 2 |
| SP2 | CLK Low time | 7 | | Tc(FIM) | |
| SP3 | CLK High time | 7 | | Tc(FIM) | |
| SP4 | Data Input setup to CLK (rx edge) | 30 - Tc(FIM) | | nS | 1 |
| SP5 | Data Input hold to CLK (rx edge) | Tc(FIM) - 5 | | nS | 1 |
| SP6 | CLK (tx edge) to Data Output | -2 | 2 | nS | 2, 3, 4 |
| SP7 | CLK (tx edge) to Chip Select inactive | 2 | | Tc(FIM) | 1, 2 |

**Note:**

**1** Tc(FIM) is the cycle time of the master FIM clock.

**2** There is an internal CLK (tx edge) even if it is not apparent on the CLK pin. This is why only the timing between the Chip Select and CLK (tx edge) is specified. Timing for the CLK (rx edge) can be derived from this timing.

**3** The CLK (tx edge) and Data Output are changed on the same master FIM clock edge, so there is a race to the output pins between these two signals.

**4** Assumes equal loading on the CLK and Data Output signals.

## FIM SPI Clock Rates

The AHB clock rate determines what SPI clock rates the FIM SPI driver can support. The AHB clock rate is normally determined by hardware strapping (see the "PLL configuration" section on page 127). The maximum SPI clock rate the FIM SPI driver can achieve is:

Maximum SPI clock rate = 4*AHB clock rate/14

**Note:** The AHB clock rate used for this calculation is not affected by the values of CSC or Max CSC in the Clock Configuration register in the System Control Module.

For example, if the AHB clock rate is 56.2176 MHz, then the maximum SPI clock rate would be 16.06217143 MHz.

The FIM SPI driver allows users to set lower clock rates. The driver sets a clock rate by setting a delay count to a value between 0 and 255. The maximum clock rate is selected when the count is 0. For values between 1 and 255, the clock rate is determined by the following formula:

SPI clock rate = (4*AHB clock rate)/(16 + delay count)

For example, if the AHB clock rate is 56.2176 MHz and the delay count is 10, then the SPI clock rate will be 2.958821 MHz.

Please note that the SPI driver API abstracts most of the configuration details. The user specifies the desired SPI clock rate and the driver sets the delay count so that the SPI clock rate is as high as possible, but not greater than 1.0125 times the specified rate.

# Change Log

## Revision A

- Initial Release