ConnectCore MP2 Dev Board

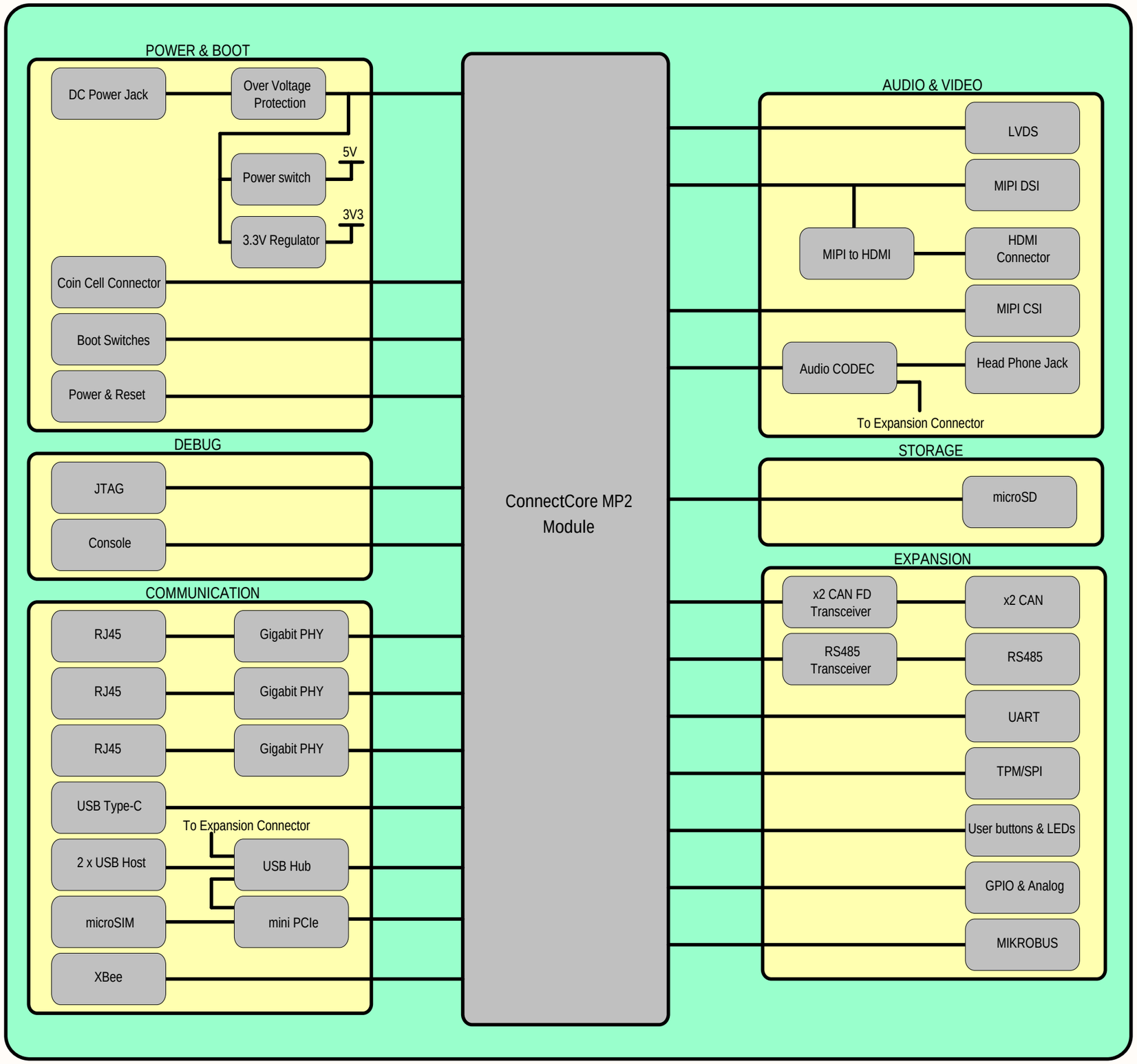


Table of Content

Title: Block Diagram	
Designer: Juan Anzola	Sheet: 1 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

ConnectCore MP2 Module

3V3 capable of supplying 2.5A. It only powers the Wireless module inside the SOM.

VCC_LICELL (pad F22 of the SOM) must be tied to VDDIO if no external battery is connected.

LDO8 is used internally on the SOM to power the SDMMC1 (wireless SDIO) I/O supply. It is externally available only in non-wireless variants of the SOM.

PI8/LPO32 not available in wireless variants of the module. This pin is used internally to clock the WLAN/BT chip.

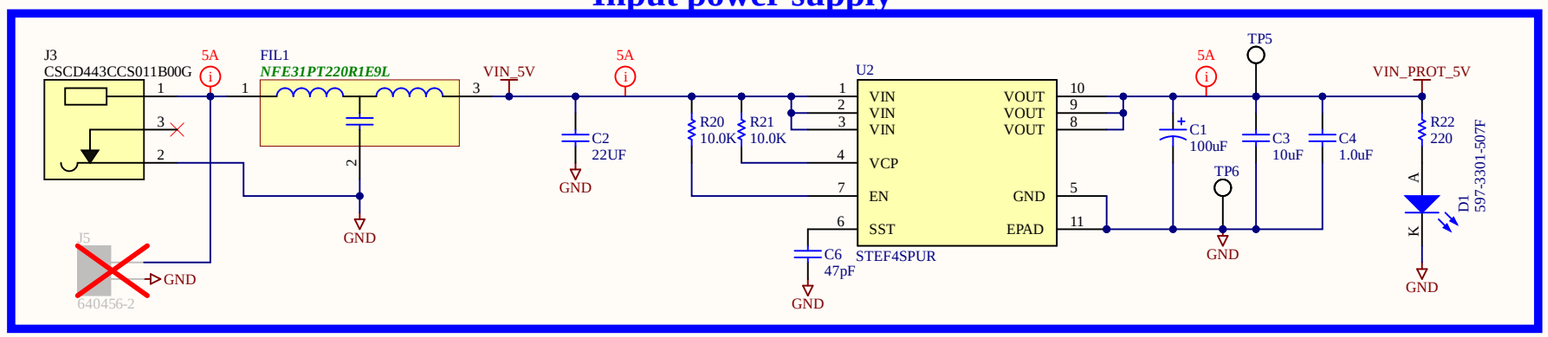
Resistors to selectd between ETH3 PHY (only available in MP257) or expansion header.

Resistors to give access to the QSPI interface on J16.

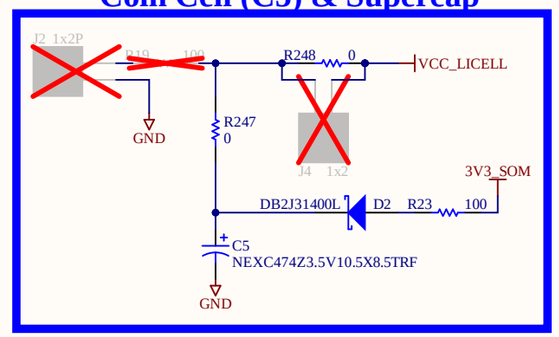
TPM_SPI is connected to internal Flash-memory-based trusted platform module. By default, this internal memory is controlled by I2C. Driving TPM_SPI_I2C externally allows to swap to SPI mode.

Title: CCMP2 Module	
Designer: Juan Anzola	Sheet: 2 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

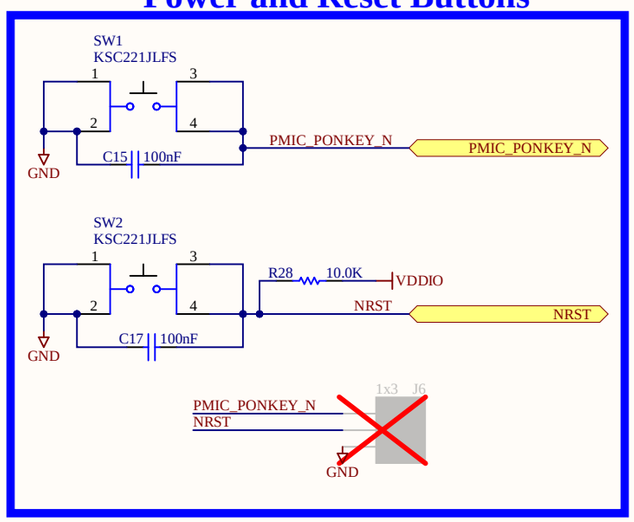
Input power supply



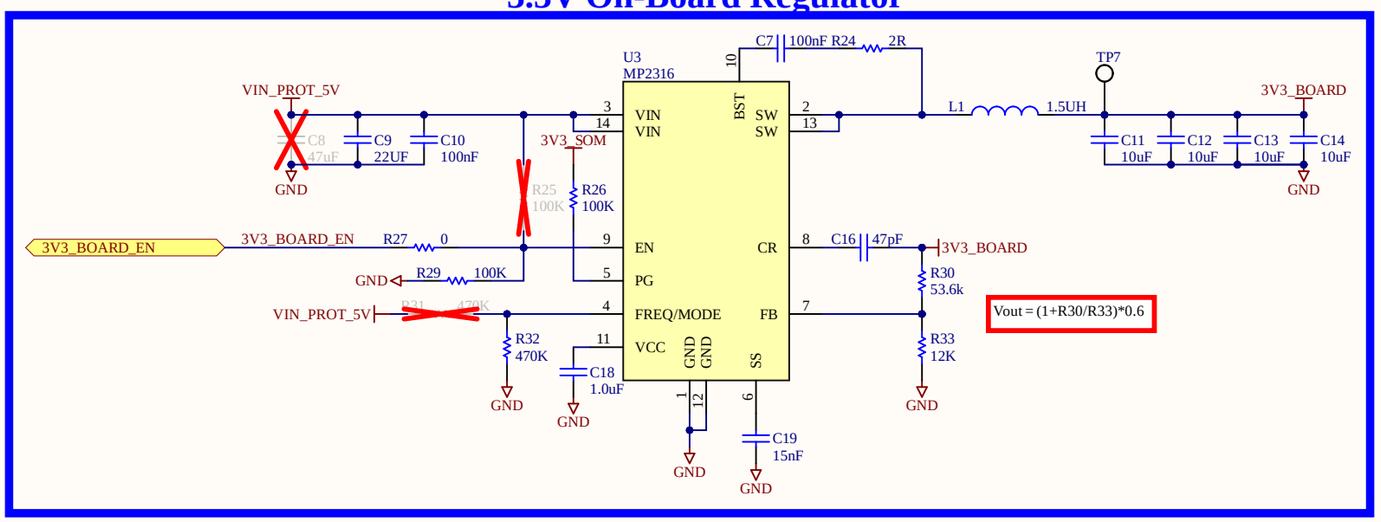
Coin Cell (C5) & Supercap



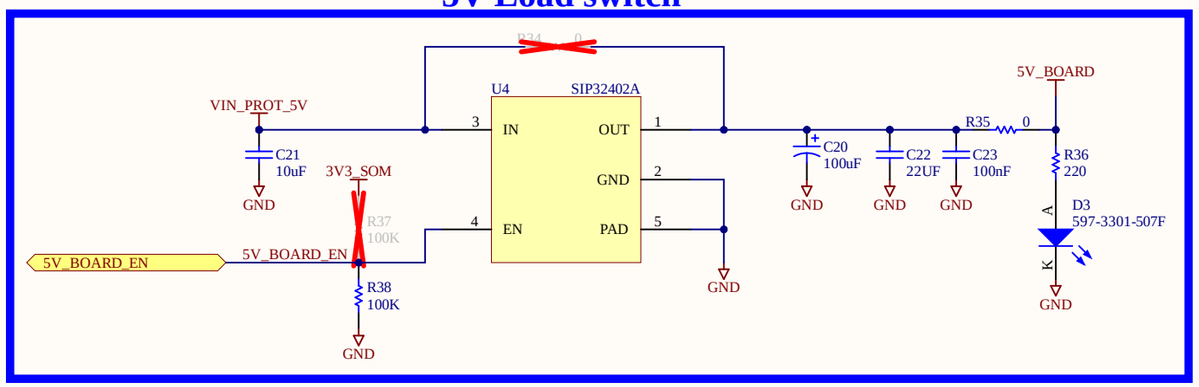
Power and Reset Buttons



3.3V On-Board Regulator

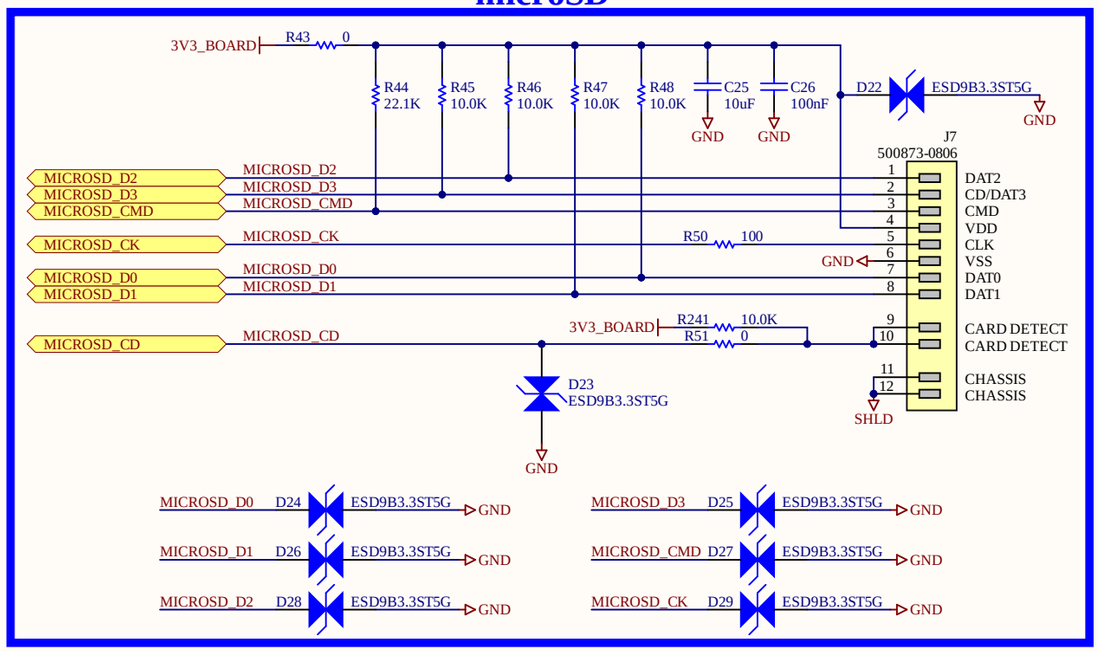


5V Load switch

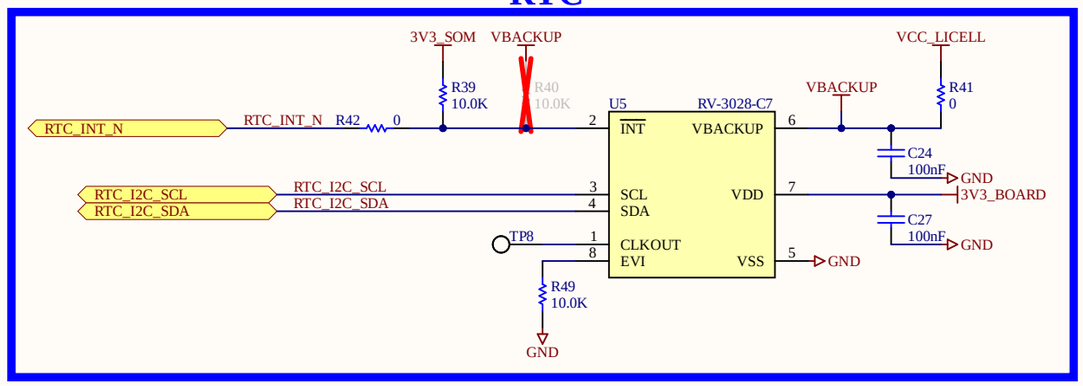


Title: Power, Reset		
Designer: Juan Anzola	Sheet: 3 of 17	
Variant: 55002225-01	Rev: 04	
Description: ConnectCore MP1 Development board - CCMP2		

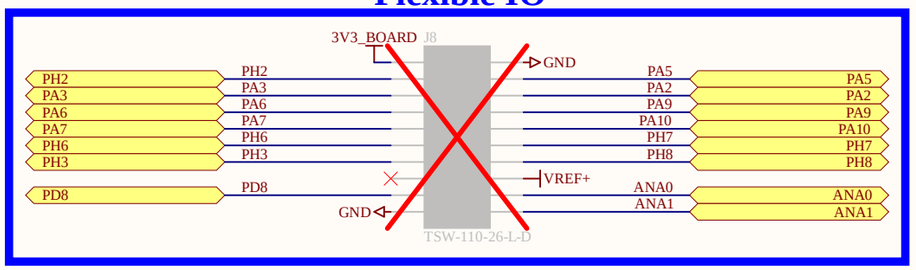
microSD



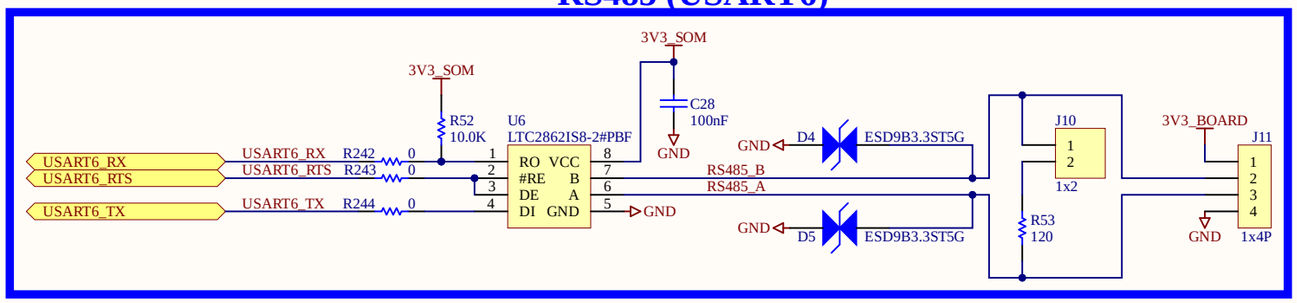
RTC



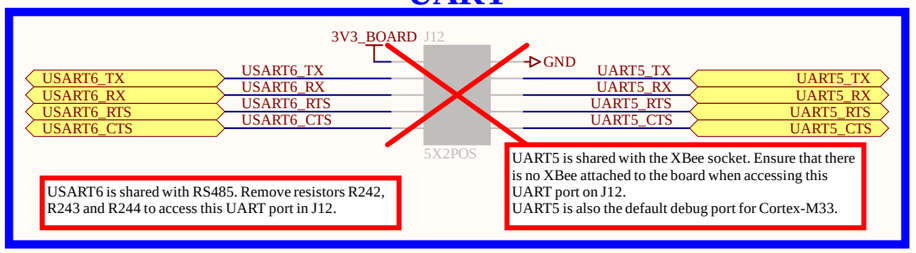
Flexible IO



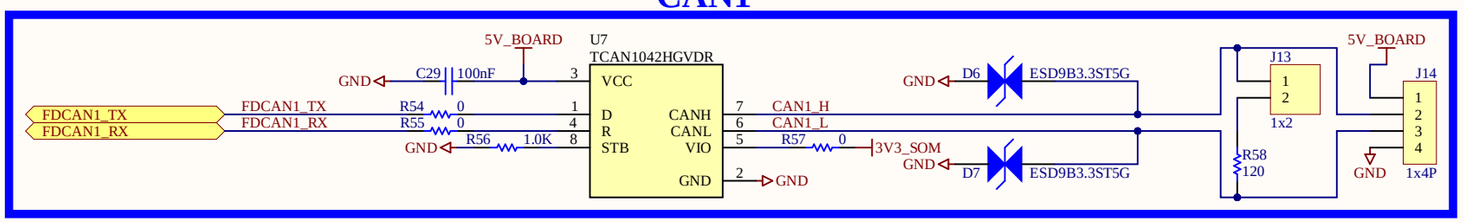
RS485 (USART6)



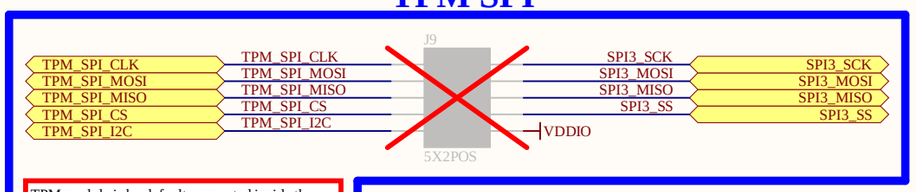
UART



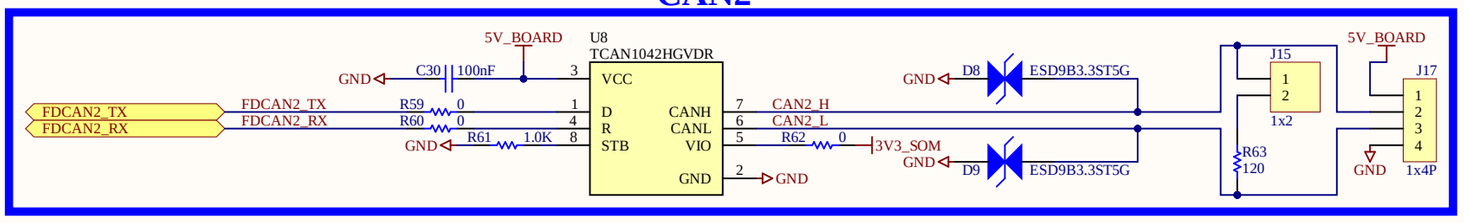
CAN1



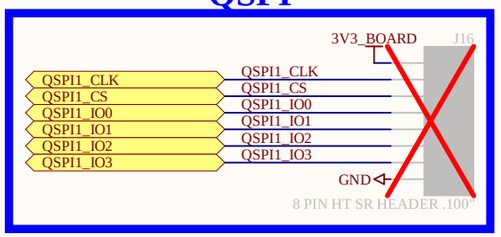
TPM SPI



CAN2

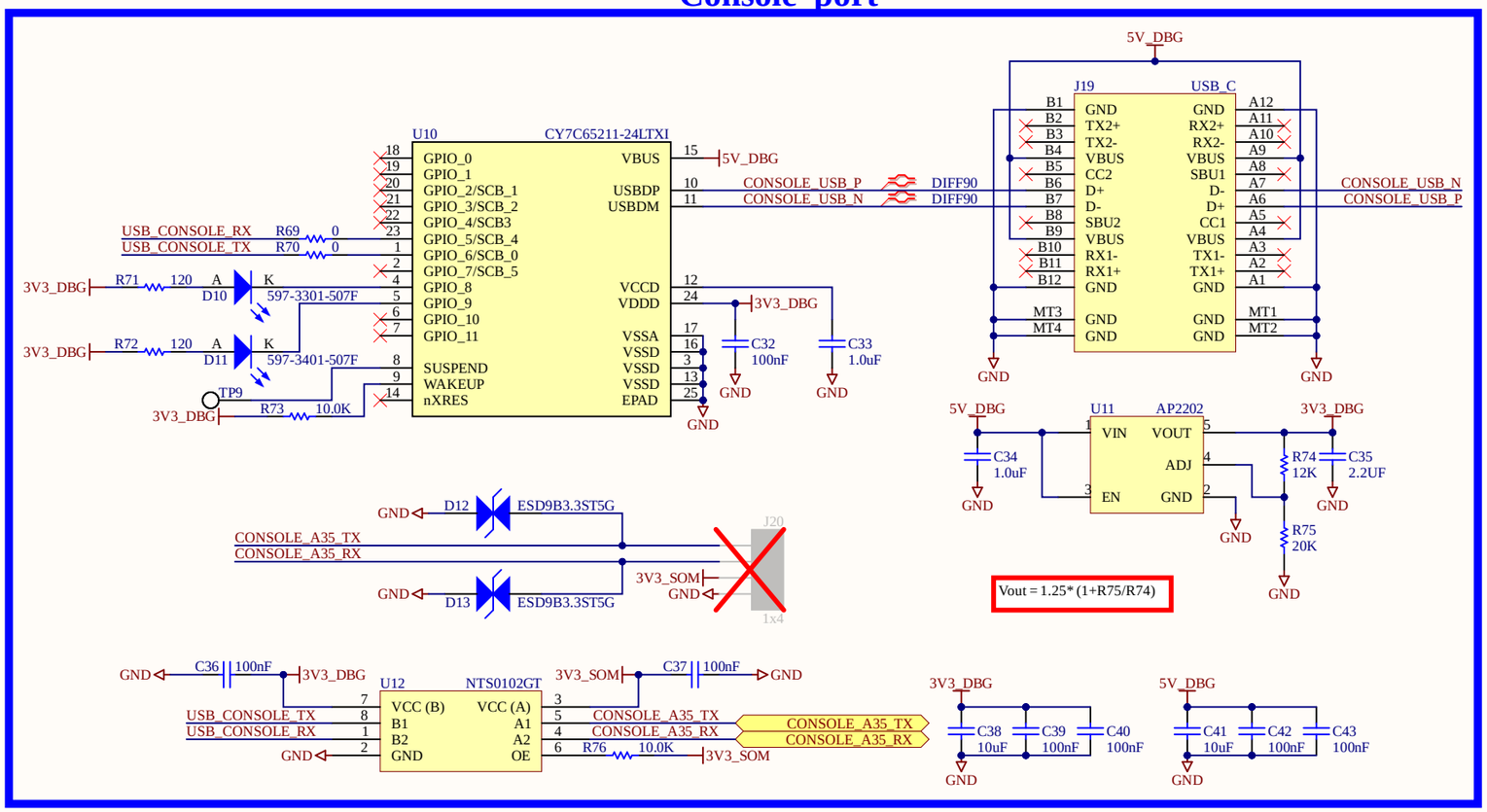


QSPI

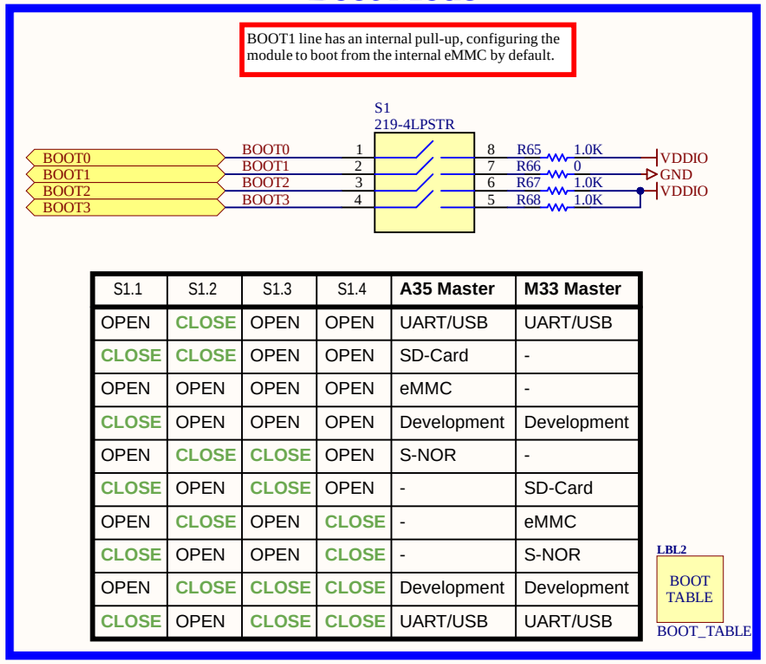


Title: MicroSD, RS485, CAN, RTC, Expansion	
Designer: Juan Anzola	Sheet: 4 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

Console_port

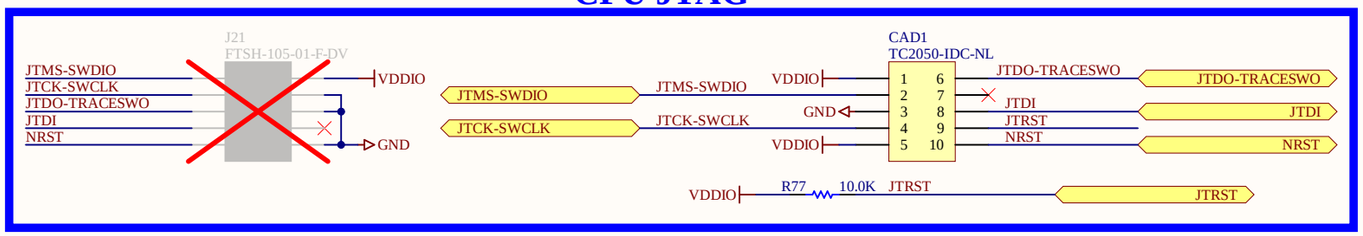


Boot Mode



S1.1	S1.2	S1.3	S1.4	A35 Master	M33 Master
OPEN	CLOSE	OPEN	OPEN	UART/USB	UART/USB
CLOSE	CLOSE	OPEN	OPEN	SD-Card	-
OPEN	OPEN	OPEN	OPEN	eMMC	-
CLOSE	OPEN	OPEN	OPEN	Development	Development
OPEN	CLOSE	CLOSE	OPEN	S-NOR	-
CLOSE	OPEN	CLOSE	OPEN	-	SD-Card
OPEN	CLOSE	OPEN	CLOSE	-	eMMC
CLOSE	OPEN	OPEN	CLOSE	-	S-NOR
OPEN	CLOSE	CLOSE	CLOSE	Development	Development
CLOSE	OPEN	CLOSE	CLOSE	UART/USB	UART/USB

CPU JTAG



Title:	**Console, JTAG, Bootstrap**
Designer:	Juan Anzola
Sheet:	5 of 17
Variant:	55002225-01
Rev:	04
Description:	ConnectCore MP1 Development board - CCMP2

Gigabit Ethernet 1

U13A
88E1512-A0-NNP2C000

S_INP 1, S_INN 2, S_OUTP 4, S_OUTN 5, TXD[0] 50, TXD[1] 51, TXD[2] 54, TXD[3] 55, TX_CLK 53, TX_CTRL 56, RXD[0] 44, RXD[1] 45, RXD[2] 47, RXD[3] 48, RX_CLK 46, RX_CTRL 43, MDC 7, MDIO 8

MDIP[0] 28, MDIN[0] 27, MDIP[1] 24, MDIN[1] 23, MDIP[2] 22, MDIN[2] 21, MDIP[3] 18, MDIN[3] 17, LED[0] 14 → LED_ACT_1, LED[1] 13 → LED1_1, LED[2]/INT 12 → LED_1000_1

ETH1_TXD0, ETH1_TXD1, ETH1_TXD2, ETH1_TXD3, ETH1_GTX_CLK, ETH1_TX_CTL, ETH1_RXD0, ETH1_RXD1, ETH1_RXD2, ETH1_RXD3, ETH1_RX_CLK, ETH1_RX_CTL, ETH1_MDC, ETH1_MDIO

3V3_ETH1 — R80 4.99K

ETH1_TXRXA_P, ETH1_TXRXA_N, ETH1_TXRXB_P, ETH1_TXRXB_N, ETH1_TXRXC_P, ETH1_TXRXC_N, ETH1_TXRXD_P, ETH1_TXRXD_N

CT1 — DIFF100 ×8 — CT, TRD1+, TRD1-, TRD2+, TRD2-, TRD3+, TRD3-, TRD4+, TRD4-, GND

SHLD, SHLD1, SHLD2, D1, D2, D3, D4, YEL, GRN

LED_1000_1 — R78 120 — 3V3_ETH1

LED_ACT_1 — R79 120 — 3V3_ETH1

J22 RJ45

CT1 — C44 100nF, C45 100nF, C46 100nF, C47 100nF — GND

FOR 88E1512PB only:

CONFIG pin configures two bits, whose value depends on what is connected to this pin after deassertion of hardware reset:
- VSS -> 00
- LED[0] -> 01
- LED[1] -> 10
- LED[2] -> Unused
- VDDO -> 11

The two bits configured through the CONFIG pin are mapped as follows:
- 00 -> PHYAD[0] 0 VDDO_LEVEL = 3.3V
- 01 -> PHYAD[0] 1 VDDO_LEVEL = 3.3V
- 10 -> PHYAD[0] 0 VDDO_LEVEL = 2.5V
- 11 -> PHYAD[0] 1 VDDO_LEVEL = 2.5V

ETH1_RXD0, ETH1_RXD1, ETH1_RXD2, ETH1_RXD3, ETH1_RX_CTL — R81 4.7K, R82 4.7K, R83 4.7K, R84 4.7K, R85 4.7K — GND

PHYAD[3:0] = 0000

FOR 88E1512PB only:

RXD[3:0] and RX_CTRL pins are also used for configuration. These pins have internal pull-ups so by default a high value is sampled. To set a low level, an external 4.7k pull-down resistor is required.
Mapping of these pins is as follows:
- RX_CTRL = 1 -> RGMII
- RX_CTRL = 0 -> MII
- RXD[0] = 1 -> MDIO
- RXD[0] = 0 -> TWSI
- RXD[3:1] -> configures PHYAD[3:1]

Note that polarity for PHYAD is reversed. A floating pin (with internal pull-up) configures a "0", while an external pull-down configures a "1".

U13B
88E1512-A0-NNP2C000

CONFIG 15 ← R86 0 (GND / LED_ACT_1 / LED1_1 / LED_1000_1 / 3V3_ETH1) → CONFIG_1

CLK125 9 ← R91 0 ← ETH1_CLK125

RESET 16 ← ETH1_RST

XTAL_IN 34 ← C57 33pF, X1 RH100-25.000-20-EXT-TR (pins 2, 4 GND), C60 33pF — GND

XTAL_OUT 33

HSDACP 32, HSDACN 31

TSTPT 29

RSET 30 ← R93 4.99K

REG_IN 36, AVDD33 20, AVDD33 25 — L2 120 — 3V3_ETH1 — C48 100nF, C49 10uF — GND

AVDD33 25 — L3 120 — C50 100nF, C51 100nF, C52 10uF — GND

VDDO 11, VDDO 49, VDDO 52, VDDO 10 → GND — L4 120 — 3V3_ETH1 — C53 100nF, C54 100nF, C55 100nF, C56 10uF — GND

AVDD18_OUT 39 — 1V8_PHY1

AVDDC18 35 — L5 120 — 1V8_PHY1 — TP10 — C58 100nF, C59 10uF — GND

AVDD18 3, AVDD18 19, AVDD18 26, AVDD18 38 — L6 120 — 1V8_PHY1 — C61 100nF, C62 100nF, C63 100nF, C64 100nF, C65 10uF — GND

DVDD_OUT 40 — 1V0_PHY1

DVDD 6, DVDD 42 — 1V0_PHY1 — TP11 — C66 100nF, C67 100nF, C68 10uF — GND

REGCAP1 37 — C69 0.22uF

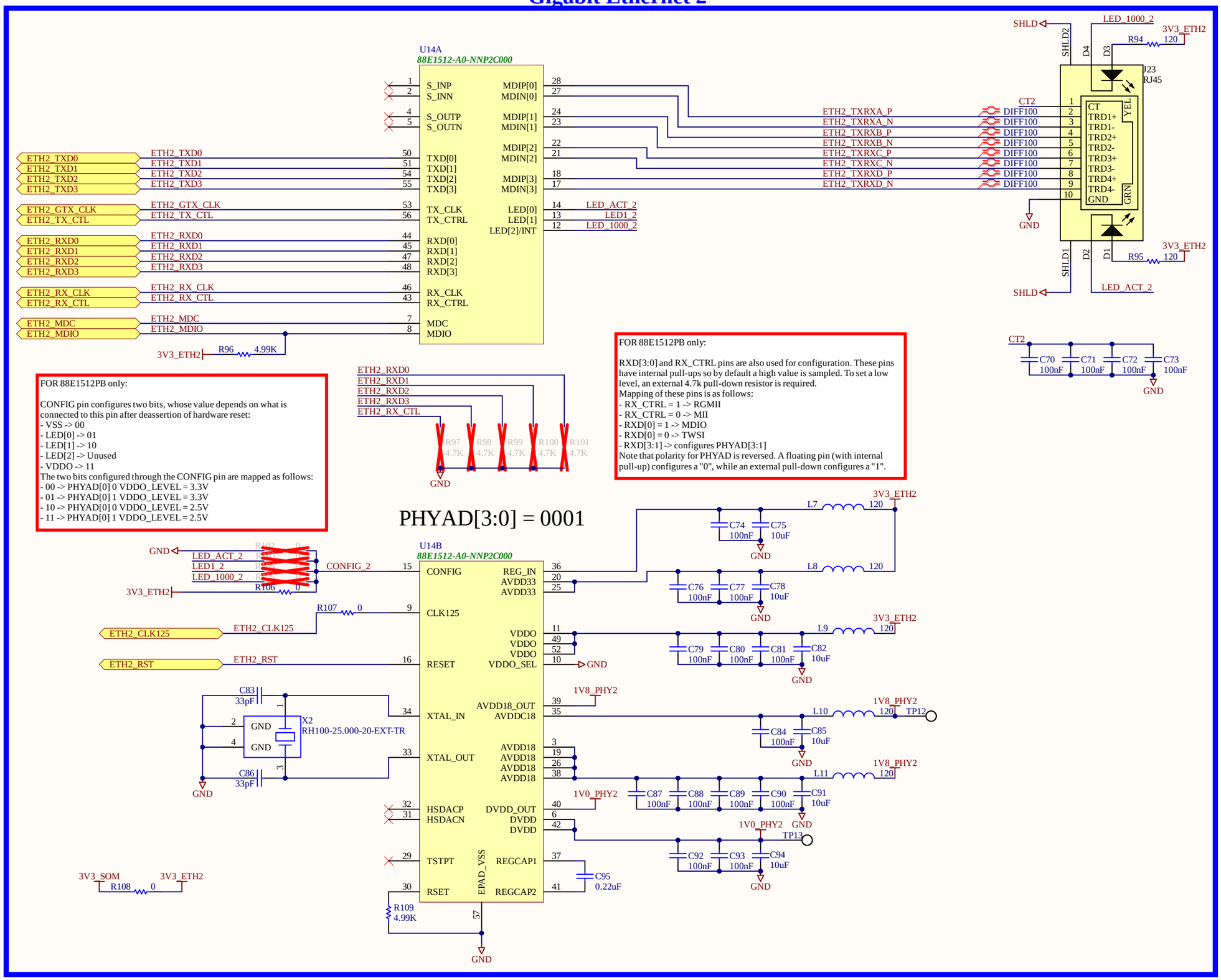
REGCAP2 41

EPAD_VSS 57 — GND

3V3_SOM — R92 0 — 3V3_ETH1

Title: Gigabit Ethernet 1	
Designer: Juan Anzola	Sheet: 6 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

Gigabit Ethernet 2



Title: Gigabit Ethernet 2	
Designer: Juan Anzola	Sheet: 7 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

Gigabit Ethernet 3 (ONLY AVAILABLE ON STM32MP257)

U15A
88E1512PB2-NNP2I000

ETH3_TXD0
ETH3_TXD1
ETH3_TXD2
ETH3_TXD3
ETH3_GTX_CLK
ETH3_TX_CTL
ETH3_RXD0
ETH3_RXD1
ETH3_RXD2
ETH3_RXD3
ETH3_RX_CLK
ETH3_RX_CTL
ETH1_MDC
ETH1_MDIO
3V3_ETH3
R112 4.99K

ETH3_TXRXA_P
ETH3_TXRXA_N
ETH3_TXRXB_P
ETH3_TXRXB_N
ETH3_TXRXC_P
ETH3_TXRXC_N
ETH3_TXRXD_P
ETH3_TXRXD_N
DIFF100

LED_ACT_3
LED1_3
LED_1000_3

SHLD
LED_1000_3
3V3_ETH3
R110 120
SHL_D2
D4
D3
J24
RJ45
CT3
GND
SHL_D1
D2
D1
R111 120
LED_ACT_3

CT3
C96 100nF
C97 100nF
C98 100nF
C99 100nF
GND

FOR 88E1512PB only:

CONFIG pin configures two bits, whose value depends on what is connected to this pin after deassertion of hardware reset:
- VSS -> 00
- LED[0] -> 01
- LED[1] -> 10
- LED[2] -> Unused
- VDDO -> 11

The two bits configured through the CONFIG pin are mapped as follows:
- 00 -> PHYAD[0] 0 VDDO_LEVEL = 3.3V
- 01 -> PHYAD[0] 1 VDDO_LEVEL = 3.3V
- 10 -> PHYAD[0] 0 VDDO_LEVEL = 2.5V
- 11 -> PHYAD[0] 1 VDDO_LEVEL = 2.5V

ETH3_RXD0
ETH3_RXD1
ETH3_RXD2
ETH3_RXD3
ETH3_RX_CTL
R113 4.7K
R114 4.7K
R115 4.7K
R116 4.7K
R117 4.7K
GND

FOR 88E1512PB only:

RXD[3:0] and RX_CTRL pins are also used for configuration. These pins have internal pull-ups so by default a high value is sampled. To set a low level, an external 4.7k pull-down resistor is required.
Mapping of these pins is as follows:
- RX_CTRL = 1 -> RGMII
- RX_CTRL = 0 -> MII
- RXD[0] = 1 -> MDIO
- RXD[0] = 0 -> TWSI
- RXD[3:1] -> configures PHYAD[3:1]

Note that polarity for PHYAD is reversed. A floating pin (with internal pull-up) configures a "0", while an external pull-down configures a "1".

PHYAD[3:0] = 0010

GND
LED_ACT_3
LED1_3
LED_1000_3
CONFIG_3
R118 0
R119 0
R120 0
3V3_ETH3

U15B
88E1512PB2-NNP2I000

ETH1_RST
ETH3_RST
R123 0
R124 0
C94 12pF
C95 12pF
X3
RH100-25.000-20-EXT-TR
GND

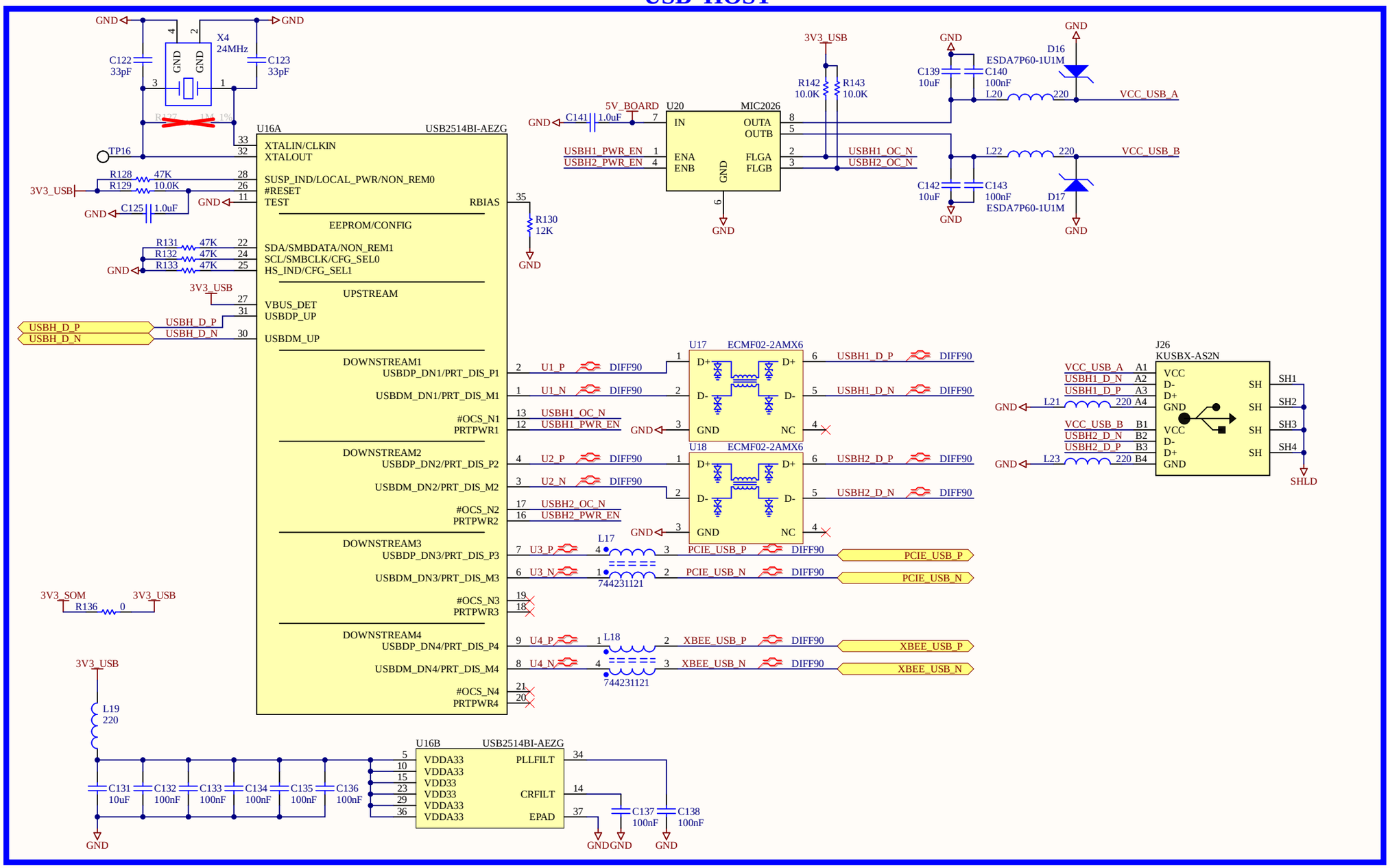
3V3_SOM
3V3_ETH3
R125 0

R126 4.99K
GND

1V8_PHY3
1V0_PHY3
TP14
TP15
C100 100nF
C101 10uF
C102 100nF
C103 100nF
C104 10uF
C105 100nF
C106 100nF
C107 100nF
C108 10uF
C110 100nF
C111 10uF
C113 100nF
C114 100nF
C115 100nF
C116 100nF
C117 10uF
C118 100nF
C119 100nF
C120 10uF
C121 0.22uF

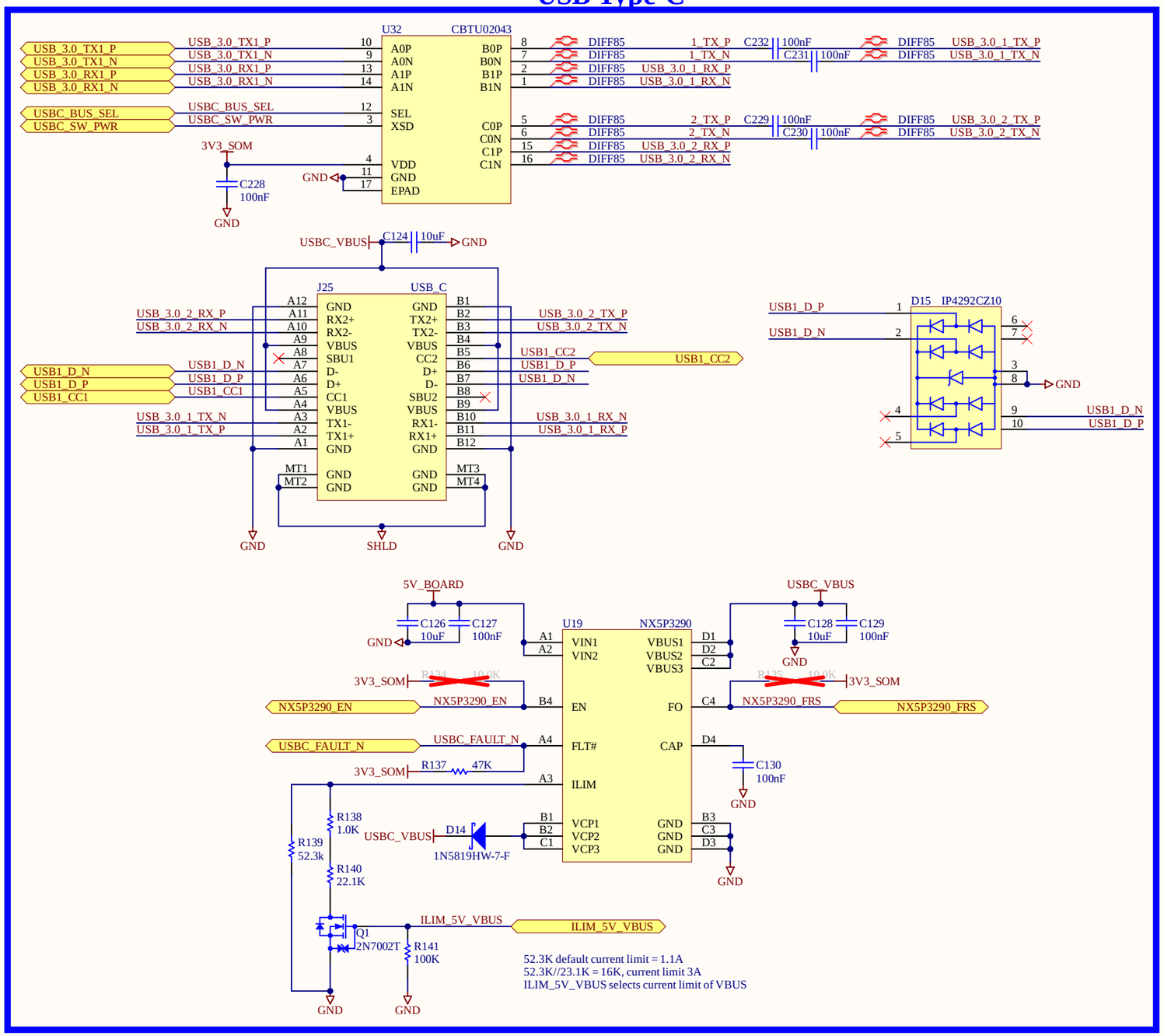
Title: Gigabit Ethernet 3	
Designer: Juan Anzola	Sheet: 8 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

USB HOST



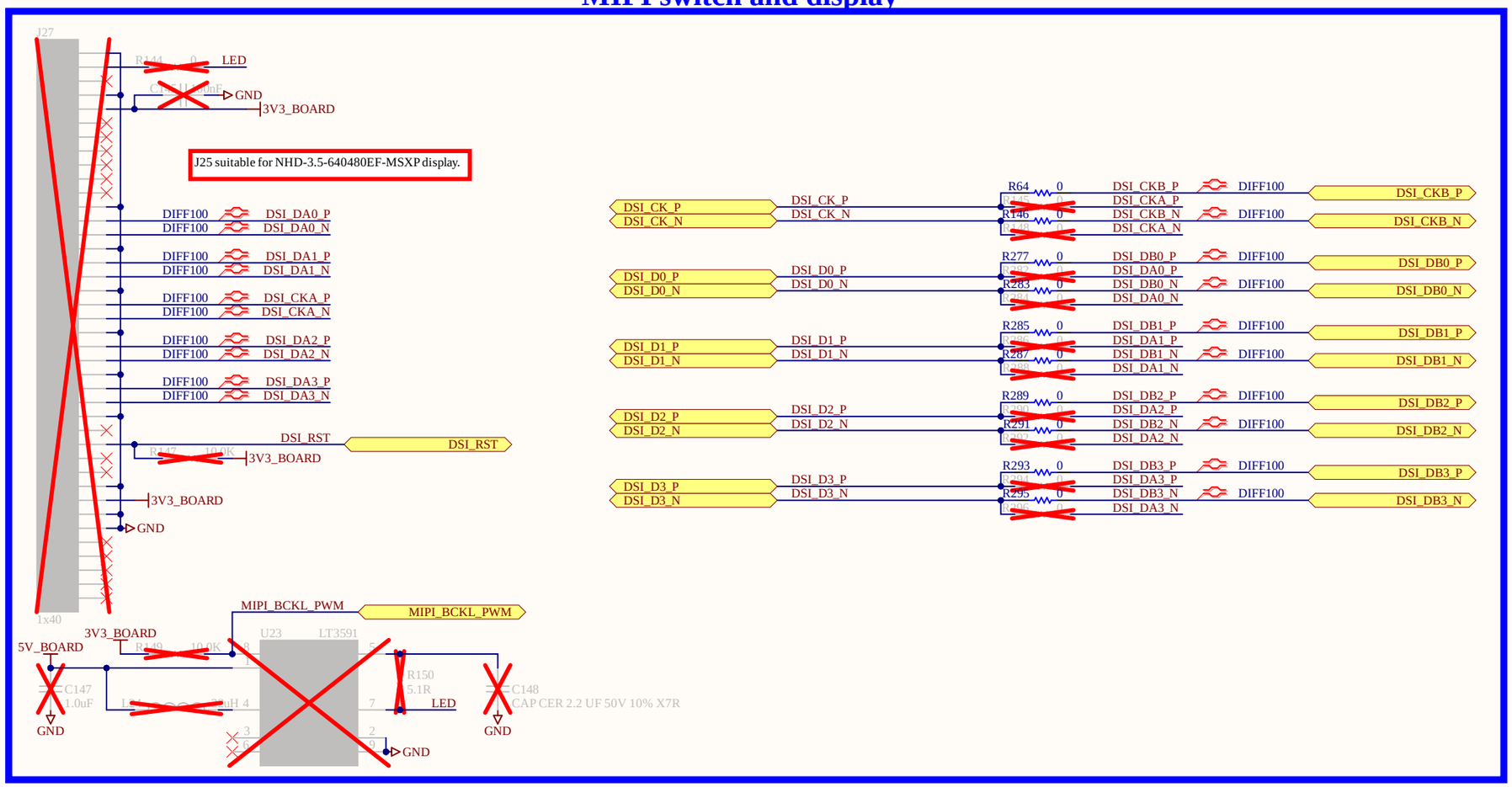
Title: USB Host	
Designer: Juan Anzola	Sheet: 9 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

USB Type-C

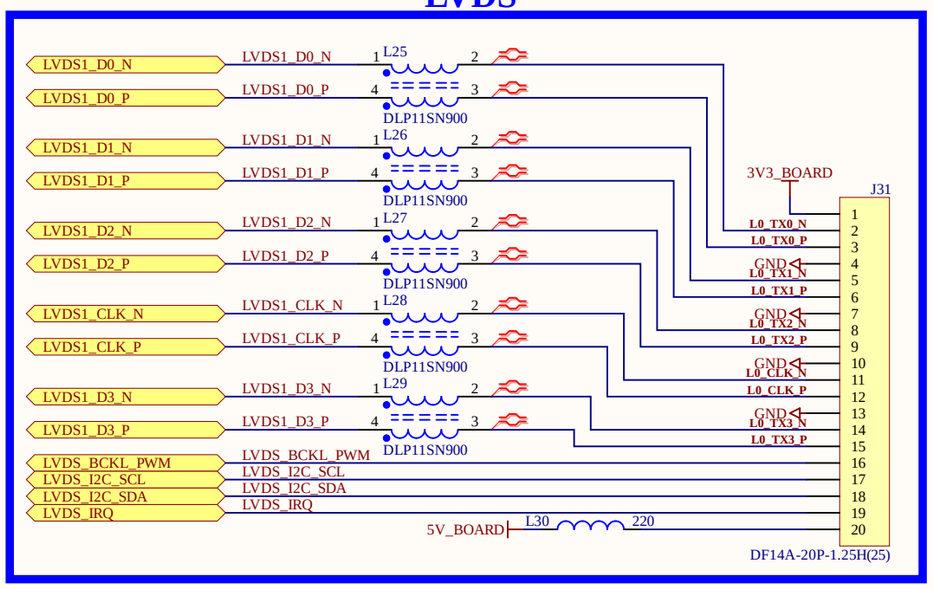


Title: USB Type-C	
Designer: Juan Anzola	Sheet: 10 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

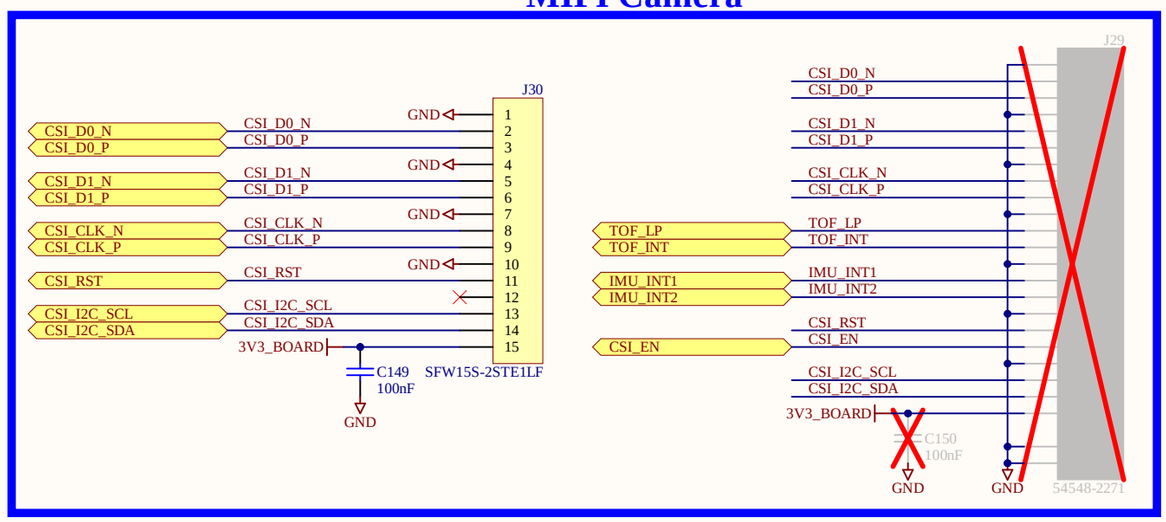
MIPI switch and display



LVDS

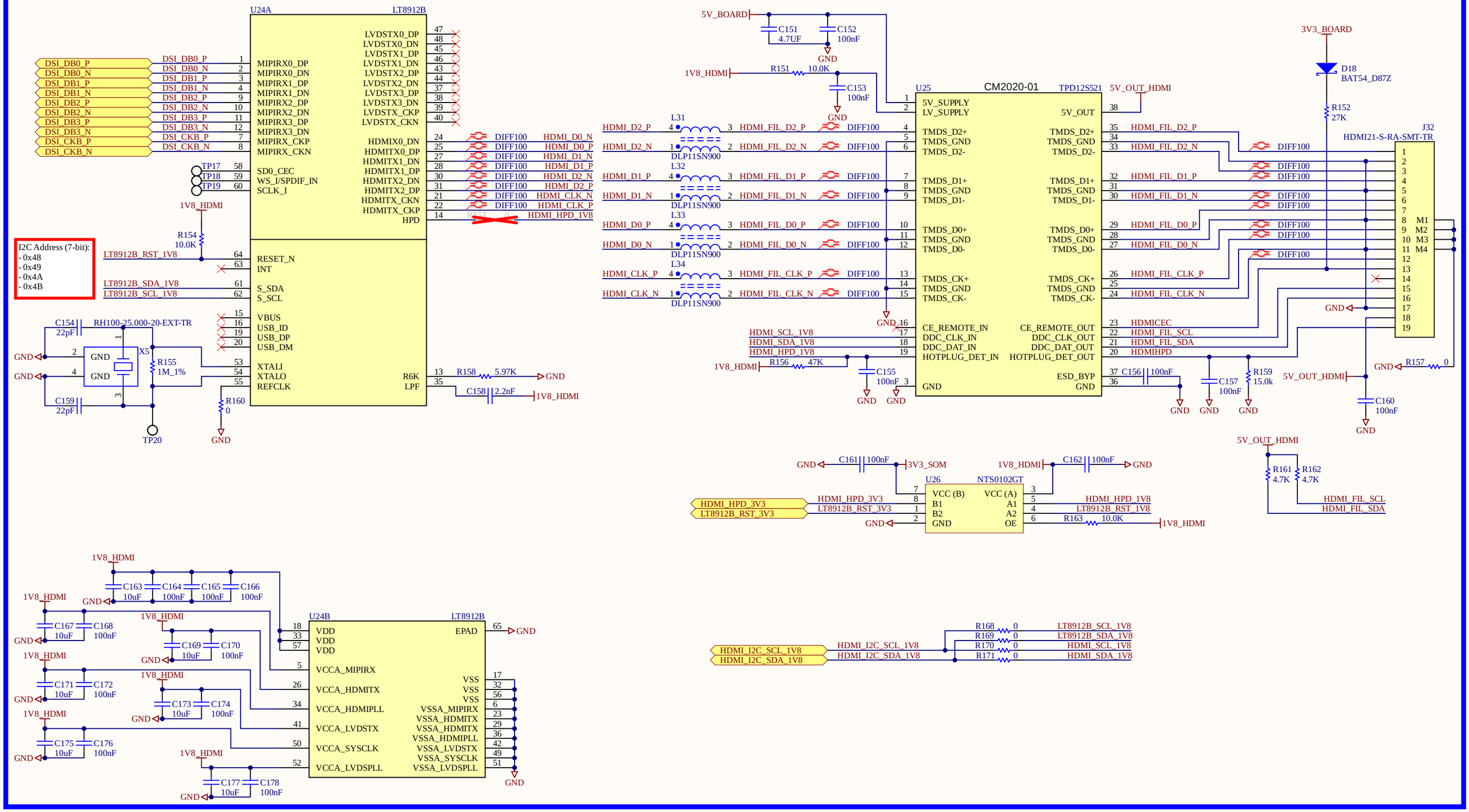


MIPI Camera



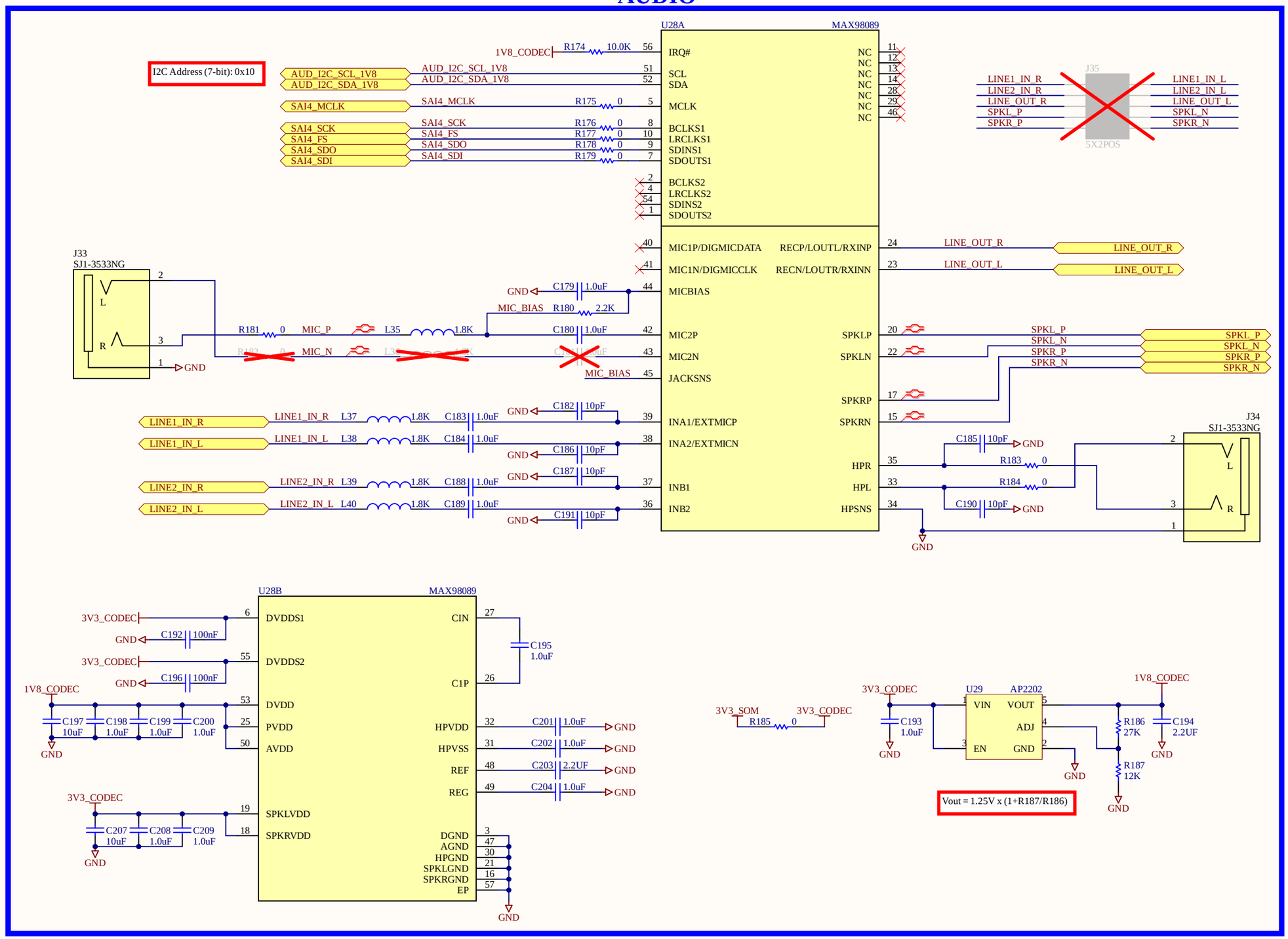
Title: MIPI Display, LVDS Display, MIPI Camera	
Designer: Juan Anzola	Sheet: 11 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

HDMI display



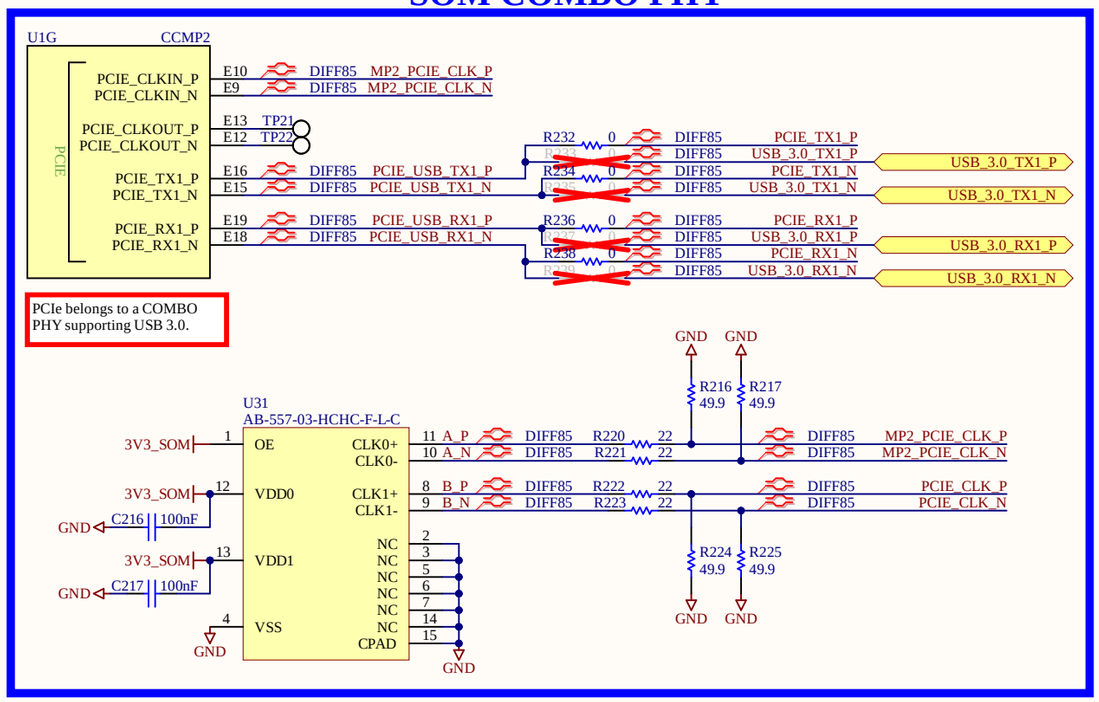
Title: HDMI	
Designer: Juan Anzola	Sheet: 12 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

AUDIO

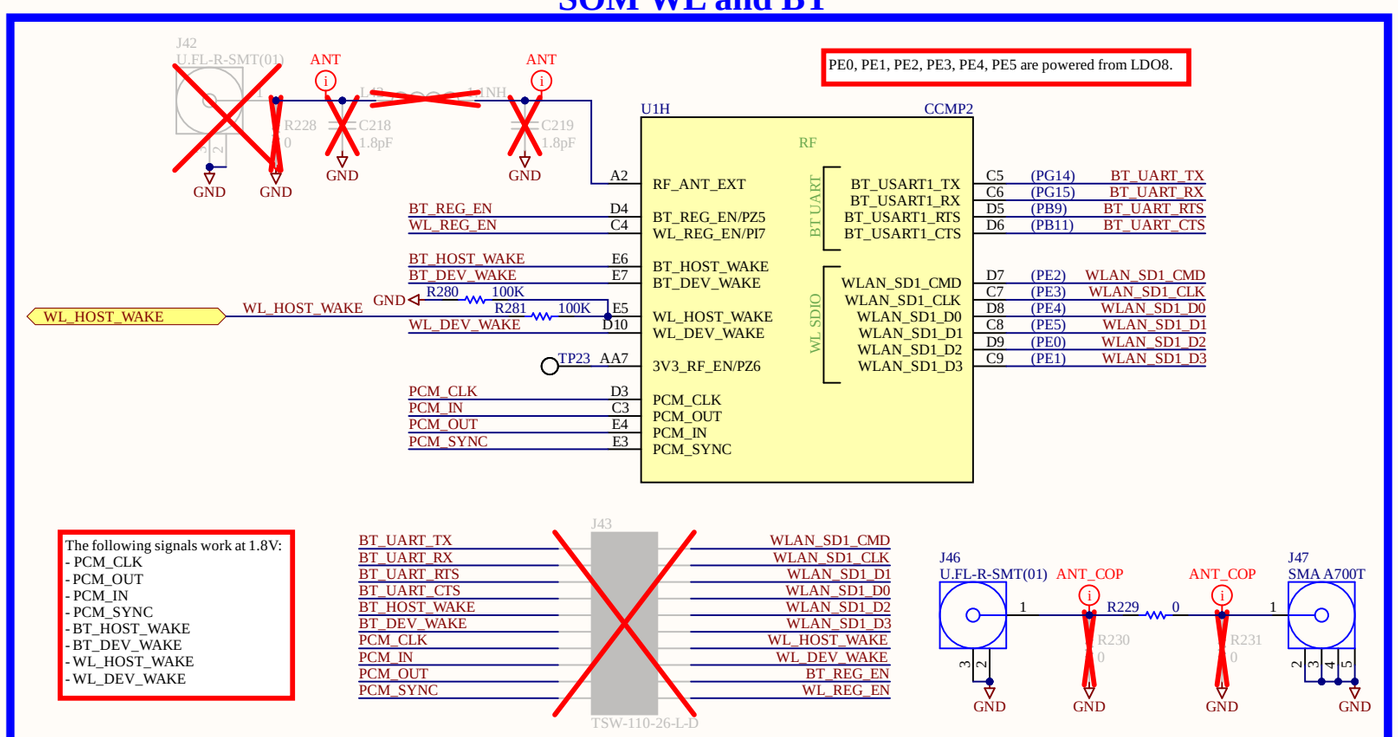


Title: Audio	
Designer: Juan Anzola	Sheet: 13 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

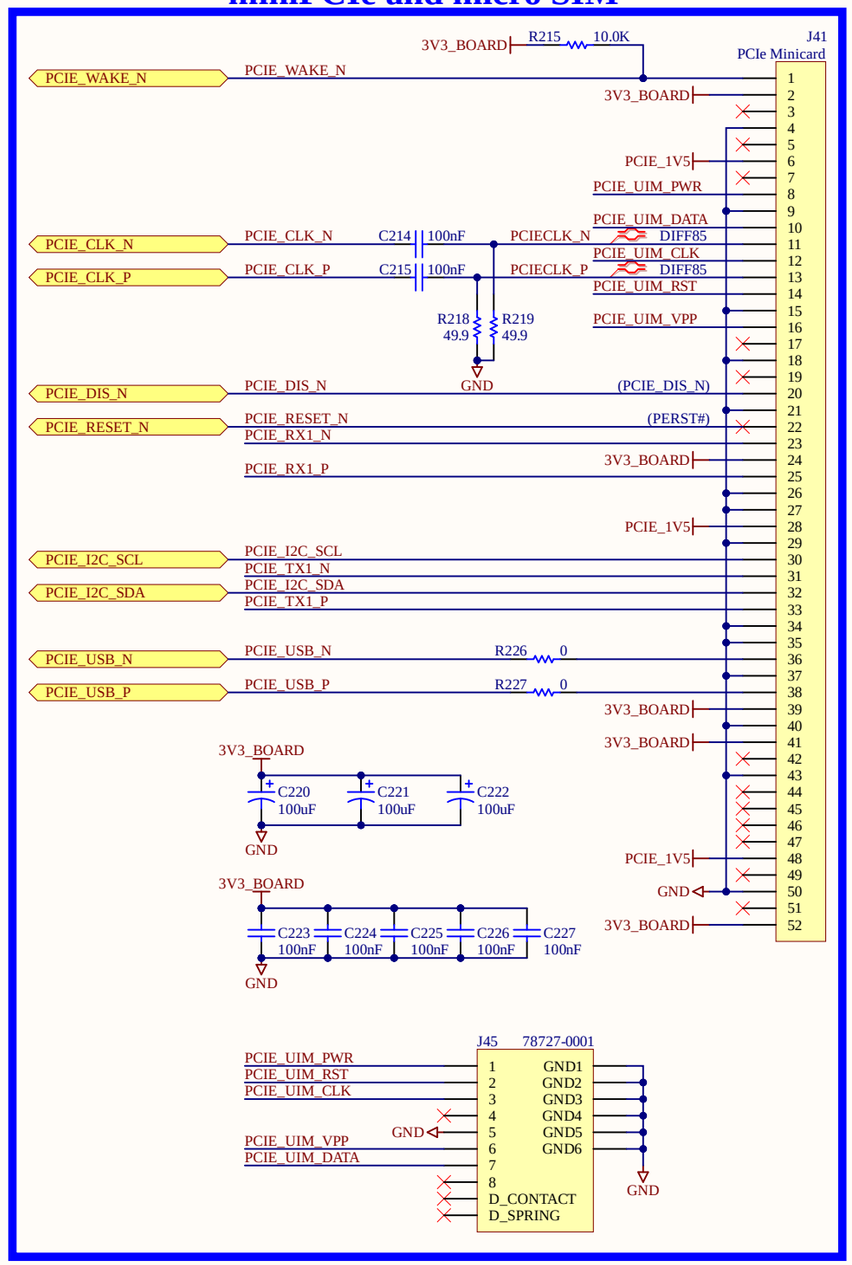
SOM COMBO PHY



SOM WL and BT

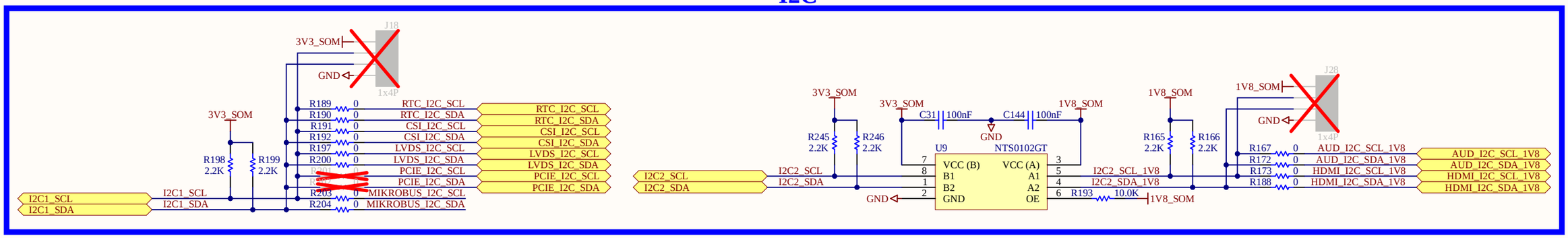


miniPCIe and micro SIM

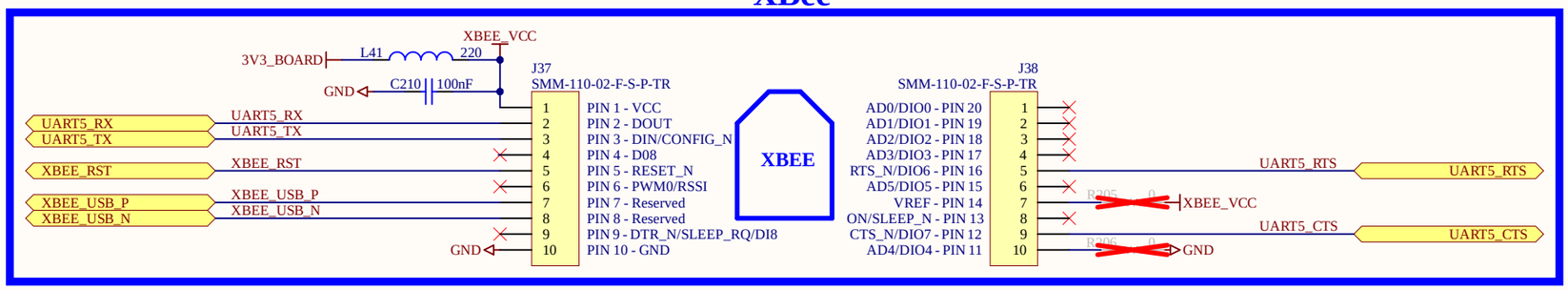


Title: RF, PCIe	
Designer: Juan Anzola	Sheet: 14 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

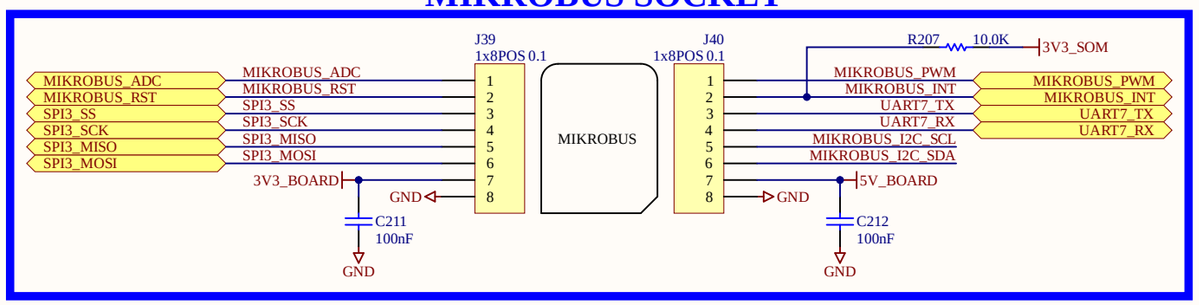
I2C



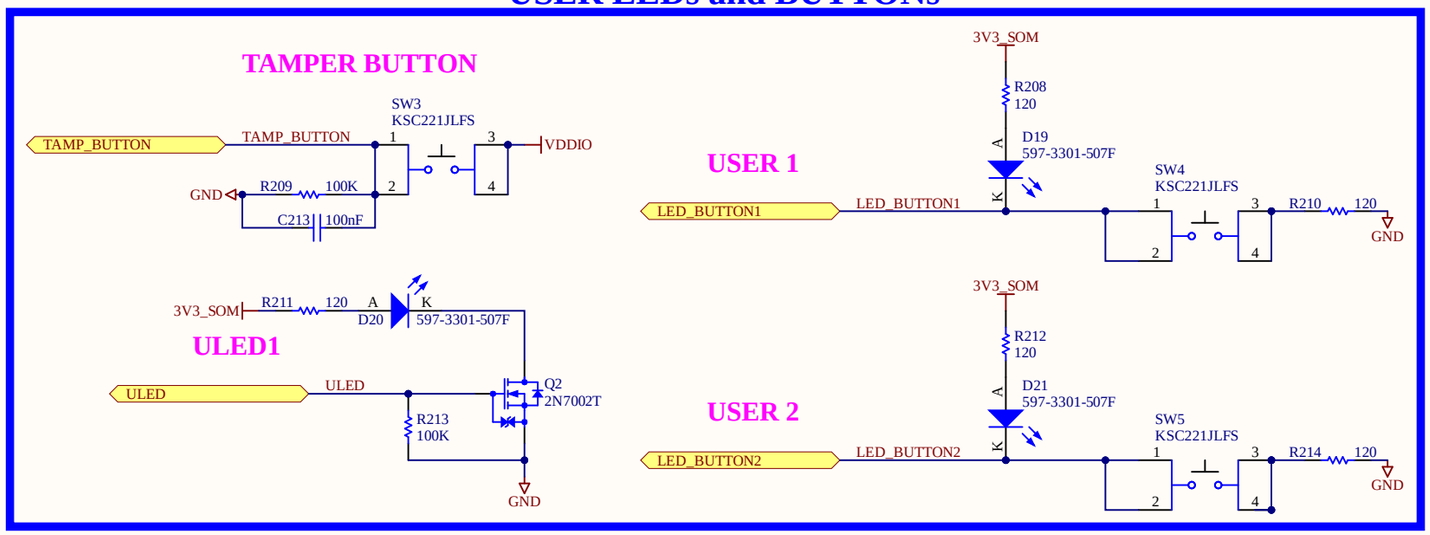
XBee



MIKROBUS SOCKET



USER LEDs and BUTTONs



Title: I2C, XBee, Mikrobus, User LEDs, Buttons	
Designer: Juan Anzola	Sheet: 15 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	

System Power Rails

Voltage (V)	Supply Name	Block	Generated by	Output current (mA)	Notes
5.0	VIN_5V	Overvoltage Prot	External DC supply	-	
	VIN_PROT_5V	CCMP2	Overvoltage Prot	-	
		3.3V Regulator			
		5V load switch			
	5V_BOARD	CAN1, CAN2	SIP32401A (U4)	2400	
		USB Type-A ports			
		USB Type-C port			
		MIPI Display			
		LVDS			
		HDMI			
		Mikrobus			
3.3	3V3_SOM	RS485	PMIC BUCK7	2500	Used also inside the SOM
		Gigabit Ethernet			
		USB Hub			
		AUDIO			
	3V3_BOARD	MicroSD	MP2316 (U3)	3000	
		PCIe minicard			
		MIPI Camera			
		MIPI Display			
		LVDS			
		XBee			
		Mikrobus			
3.0	VCC_LICELL	RTC	External Coin Cell	-	
1.8	1V8_CODEC	AUDIO	AP2202 (U29)	150	
	1V8_HDMI	HDMI	PMIC LDO7	-	
1.5	PCIE_1V5	PCIe minicard	PMIC LDO6	-	

GPIO Table

Signal Name	GPIO
3V3_BOARD_EN	PA12
5V_BOARD_EN	PB3
CSI_EN	PF3
CSI_RST	PG7
DSI_RST	PD7
ETH1_RST	PB2
ETH2_RST	PG6
ETH3_RST	PB15
HDMI_HPD_3V3	PD2
ILIM_5V_VBUS	PZ8
IMU_INT1	PZ0
IMU_INT2	PZ1
LED_BUTTON1	PF10
LED_BUTTON2	PF12
LT8912B_RST_3V3	PD4
LVDS_BCKL_PWM	PB0
LVDS_IRQ	PD5
MICROSD_CD	PI6
MIKROBUS_ADC	PG1
MIKROBUS_INT	PG3
MIKROBUS_PWM	PF11
MIKROBUS_RST	PG2
MIPI_BCKL_PWM	PD9
NX5P3290_EN	PG4
NX5P3290_FSR	PB6
PCIE_DIS_N	PH4
PCIE_RESET_N	PH5
PCIE_WAKE_N	PA1
RTC_INT_N	PF4
TAMP_BUTTON	PZ2
TOF_INT	PZ7
TOF_LP	PZ4
ULED	PF5
USBC_BUS_SEL	PD11
USBC_FAULT_N	PZ9
USBC_SW_PWR	PD10
WL_HOST_WAKE	PZ3
XBEE_RST	PD6

Interrupts Usage

IO index	Interrupt
0	PA0*
1	
2	
3	PG3/PZ3
4	
5	PD5
6	
7	
8	
9	PZ9
10	PF10
11	
12	PF12
13	
14	
15	

*Used inside the SOM

Title: GPIO Table, System Power Rails
Designer: Juan Anzola
Sheet: 16 of 17
Variant: 55002225-01
Rev: 04
Description: ConnectCore MP1 Development board - CCMP2

Format: DD/MM/YYYY

23/04/2024 - CCMP2 Development Board
* Revision: 01
- Initial version

23/05/2024 - CCMP2 Development Board
* Revision: 02
- No changes

03/06/2024 - CCMP2 Development Board
* Revision: 03
- No changes

21/06/2024 - CCMP2 Development Board
* Revision: 04
- PCB spin: 3001797x-01 rev A -> 3001797x-02 rev A

LBL1

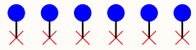
LABEL

28000351_LABEL

TXT1

LABEL
TEXT

95015873



Title: History, Mechanicals	
Designer: Juan Anzola	Sheet: 17 of 17
Variant: 55002225-01	Rev: 04
Description: ConnectCore MP1 Development board - CCMP2	