Specification Developers Kit & Dev Board A9M9750_2

ModARM9 with Netsilicon NS9750/NS9360 CPU

17. October 2005

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Table of Contents:

1. History

Date	Version	Responsible	Description
05.10.2005	0.90	K Rudolf/D. Fögele	Chapter 2.1 “Board Changes from A9M9750DEV_1 to A9M9750DEV_2” added. Signal names RIN changed in RI (signal Ring Indicator)
17.10.2005	0.99	K Rudolf	Spec adapted to layout reality

2. Overview

The A9M9750 Developer's Kit consists of the module A9M9750 inserted in a base board, LCD with adapter board, cabling, documentation and software. Two A9M9750 Developer's Kits are planned: one for Linux (LxNETES v3.0) and one for Windows CE .NET 4.2.

The A9M9360 Developer's Kit consists of the module A9M9360 inserted in a base board, LCD with adapter board, cabling, documentation and software. Two A9M9360 Developer's Kits are planned: one for Linux (LxNETES v3.0) and one for Windows CE .NET 4.2.

3. Market Requirements

The various ARM-based SoCs that are now available typically address specific market segments. It is now relatively easy for companies who are silicon market leaders in a niche segment to add an ARM core to their silicon and so provide a single chip solution reducing cost and complexity to their end customers. A typical example of this is the Micrel KS8695 which has been designed as a residential gateway for SOHO applications.

Although the ARM-based SoCs have been designed for a particular market, it does not mean that a module with this SoC on it should address the same market. So the markets we want to address with ModARM9 modules are still the ones where we have been successful in the past. The NetSilicon module will target applications requiring a GUI with an Ethernet connection and be able to do this competitively. This means that the following markets can be addressed:

- Industrial automation
- Retail point-of-sale
- Medical equipment

The emphasis on the GUI will probably mean that Linux and Windows CE .NET will be popular on the A9M9750 and the A9M9360, where Linux has it strength in networking applications.

4. Features of the Base Board

The base board will contain the following components and interfaces:

- 5.7” TFT display (SHARP) with touch screen controlled by SPI
- RJ45 ethernet connector and transformer for 100MBit/s, with integrated LEDs
- 4 serial interfaces realized with an external quadruple UART or by FPGA on board
- 1 serial channel switchable to IrDA mode with IrDA converter and transceiver on board
- 2 CAN channels with driver. CAN controller(s) are option in the FPGA
- Reprogramming of FPGA Configuration EEPROM either with ALTERA Byte Blaster II cable, by JTAG booster or with special update program directly from Module
- USB connectors for host and device, alternate usage with A9M9750 module, parallel usage with A9M9360 module using external USB PHY on board possible
- Mini PCI slot (unused by A9M9360 module)
- Compact Flash slot
- Audio codec (UDA1341TS) with line-out/headphone jack and connectors for microphone and line
- Connector for 5V power supply
- Generation of 3.3V for board and module
- VLIO connected to either 3.3V or 5V allows workaround for A9M9750_0 prototypes
- Socket with 3V battery cell for RTC buffering
- JTAG 20-pin connector and 8-pin JTAG Booster connector
- Connectors for the module signals (like on the A9Mvali), but realized as PC/104 press fit contacts with pin on top and acceptable on the bottom.
- Connector for TFT LCD, this is a 2row, 40pin connector.
- Reset button
- Power LEDs
- Debug LED
- Two user buttons, optionally logical ANDed with two status lines from FPGA
- 8 DIP switches for configuration

4.1. Board Changes from A9M9750DEV_0 to A9M9750DEV_1

- New sheet “Mechanics, Pseudos” in schematics added
- PCB and mechanic parts in schematics transferred from sheet “Version History” to sheet “Mechanics, Pseudos”
- Screws washers and nuts for CF connector added
- missing signal PCI_AD24 added
- Test lands at all unused FPGA pins added
- Test points at all voltages and Gnd added
- Board allows usage of A9M9750 or A9M9360 modules; name changed to A9M9750DEV_1
- 3.3V continous power supply name changed to 3.3V_IN; connected to module 3.3V power, VLIO selection and 2 FET switches TPS2022 on board
- Power sequencing added: Separate +3.3V switches for CF/PCI stage and rest of board controlled by signal PWREN from module
- Connection option between VLIO, +5V and +3.3V_IN allows workaround for A9M9750 prototype modules
- Disconnected A26 and A27 at FPGA (A26 & A27 are NC at A9M9360 module)
- Disconnected DMA1_REQ and DMA1_ACK# at FPGA (used for USB_PHY at A9M9360 module)
- External USB PHY controlled by GPIO42..48 added (USB lines 5V tolerant and 15KV ESD protected)
- Analog switches for GPIO12, 42..48 to select different USB configurations or FPGA programming mode with jumper added
- RSTIN# made bidirektional with 470R series resistor
- IDSEL of Mini-PCI socket connected with 0R to PCI_AD16 (set to PCI device 5)
- External UART changed to 16C754 (16C654 IrDA option unavailable due to wrong case and 16C754 already used at other projects)
- L3 connection audio changed from I2C to FPGA or CPLD to allow other protocol than I2C (AUD_L3_SCL to E6 = IO38_2, was connected to GPIO48 at DEV_0; AUD_L3SDA to E5 = IO39_2, was connected to GPIO2 at DEV_0)
- Audio chip U6 QMUTE grounded, OVERFL floating
- CAN Transceivers changed to 3.3V types
- CAN voltage shifting stages removed
- USB and ethernet connected to extension connectors via series resistors near X1,2
- CAN signals from module with jumpers connected to CAN channel 0
- External UART and FPGA now independent. All necessary logic in additional CPLD ispMACH4064 included to omit FPGA with external UART
- PCI arbiter patch for NS9750 in FPGA added
- Pull up resistor for IRQ2 (CPLD and FPGA logical ORed)
- Connection audio Microphone one channel connected to left channel
- 100R series resistor for ethernet activity and speed LEDs added
- GPIO46, 47 free, no longer for USB_EXTPHY_ENUM and USB_EXTPHY_SPEED used; these signals hardwired now

4.2. Board Changes from A9M9750DEV_1 to A9M9750DEV_2

- The product number is **not changed**: 376. This product change will be effective beginning with serial number 376 0101.
- AUD_WS signal routed to CPLD and FPGA instead of routed to GPIO10. This was patch on A9M9750DEV_1 and electrically identical delivered boards A9M9750DEV_1.
  - Connection AUD_WS to pin B15 CPLD U6 included, MP52 deleted
  - Connection AUD_WS to pin P2 FPGA U17 included, MP26 deleted
  - Connection GPIO10 to AUD_WS removed
- Hardware workaround for PCI arbiter bug for PCI slots 0, 2 and 3. This is a new feature, but default configuration is identical to A9M9750DEV_1.
  - PCI_REQ0# connected to P14 FPGA U17, MP35 deleted
  - PCI_REQ2# connected to P14 FPGA U17, MP35 deleted
  - PCI_REQ3# connected to P15 FPGA U17, MP36 deleted
  - SPCI_REQ0# connected to E13 FPGA U17, MP10 deleted
  - SPCI_REQ2# connected to E13 FPGA U17, MP10 deleted
  - SPCI_REQ3# connected to D14 FPGA U17, MP11 deleted
  - PCI_GNT0# connected to E14 FPGA U17, MP8 deleted
  - PCI_GNT2# connected to E14 FPGA U17, MP8 deleted
  - PCI_GNT3# connected to F12 FPGA U17, MP9 deleted
  - Bypass resistor R139 between PCI_REQ0# and SPCI_REQ0# added, default populated
  - Bypass resistor R141 between PCI_REQ2# and SPCI_REQ2# added, default populated
  - Bypass resistor R142 between PCI_REQ3# and SPCI_REQ3# added, default populated
  - SPCI_REQ0# connected to X21 pin D4 instead of signal PCI_REQ0#
  - SPCI_REQ1# connected to X20 pin A5 instead of signal PCI_REQ1#
  - SPCI_REQ2# connected to X20 pin B5 instead of signal PCI_REQ2#
  - SPCI_REQ3# connected to X21 pin C5 instead of signal PCI_REQ3#
- Signal LCD_PWREN renamed to LCD_PWREN# as this signal is used low active in our design. This is no functional modification compared to A9M9750DEV_1.
- Via with 0.55mm (under BGA) changed in solder mask. Priveously solder mask was totally opened for this Via.

- Changes in BOM/Manufacturing
  - PCB changed
  -

4.3. Usage Features vs Module and Base Bord Combinations

A9M9750DEV_0 and A9M9750DEV_1 base boards can be used with modules A9M9750_0, A9M9750_1, A9M9360_0 and A9M9360_1. All combinations are possible, but not all features can be used on all combinations.

Modules on A9M9750DEV_0:

Feature	A9M9750_0 (1)	A9M9750_1,2	A9M9360_0 (2)	A9M9360_1,2
Power Sequencing	VLIO to 5V	VLIO to 3.3V or 5V	VLIO to 3.3V or 5V	VLIO to 3.3V or 5V
External UART	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
LCD	yes	yes	yes	yes
Touch	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
USB host or device	yes	yes	yes	yes
USB host and device	not possible with NS9750	not possible with NS9750	yes	yes
Audio	no (3)	no (3)	no (3)	no (3)
Mini-PCI	needs wire PCI_IDSEL to PCI_AD11	yes	no PCI	no PCI
IP UARTs	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
IP CAN	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
Compact Flash	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
PCI arbiter patch	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA

Modules on A9M9750DEV_1:

Feature	A9M9750_0 (1)	A9M9750_1,2	A9M9360_0 (2)	A9M9360_1,2
Power Sequencing	VLIO to 5V	ok	ok	ok
External UART	yes, needs CPLD	yes, needs CPLD	yes, needs CPLD	yes, needs CPLD
LCD	yes	yes	yes	yes
Touch	yes, needs CPLD	yes, needs CPLD	yes, needs CPLD	yes, needs CPLD
USB host or device	yes	yes	yes	yes
USB host and device	not possible with NS9750	not possible with NS9750	yes	yes
Audio	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
Mini-PCI	needs wire PCI_IDSEL to PCI_AD11	yes	no PCI	no PCI
IP UARTs	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
IP CAN	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
Compact Flash	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA
PCI arbiter patch	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA	yes, needs FPGA

(1): Needs mini PCI signals changed on module (patch)

(2): Needs USB signals changed on module and strapping pin latch delay (patches)

(3): I2C signals on L3 port do not work

5. Components of the Developer's Kits

5.1. A9M9750/A9M9360 Developpers Kit LxNETES

Preliminary parts list for the A9M9750/A9M9360 Developer's Kit for LxNETES:

Article No.	Description	Quantity	Info1
364	A9M9750 module, 16MB SDRAM, 32MB NAND Flash, 8K EEPROM, 10/100Mb Ethernet	1	
or 382/383	A9M9360 module, 32/64MB SDRAM, 32/64MB NAND Flash, 8K EEPROM, 10/100Mb Ethernet		
376	A9M9750/A9M9360 Developer Board	1	
370	A9M2410/A9M9750/A9M9360 LCD Board	1	
9042	A9M9750/9360 Documentation CD	1	
9044	LxNETES v3.x for ARM9 CD	1	
90XX	JTAG Booster for NS9750/9360	1	
TN01051	Power Supply	1	
TK01117	Power adapter cable	1	
TK00053	Null Modem cable	1	

6. Detailed Specification Dev. Board

6.1. Module Signals

All module signals from A9M9750/A9M9360 are routed either to extension connectors with 2.54mm spacing allowing direct connection of measuring cables with 0.4mm connectors or to the appropriate drivers or interface connectors. Speed critical signals do have additional connections at the extension connectors with serial resistors near module connectors (Ethernet, USB) enable measuring of the signals but allow removing connection to expansion connectors if signal integrity problem occur.

6.2. FPGA

An ALTERA Cyclone I FPGA in a 256 BGA case provides additional stages: Compact Flash slot, up to 4 additional UARTs and up to two CAN channels. It is connected to the external module address and data bus and uses EXT_CS0#, EXT_CS2#, EXT_CS3#, EXT_OE# and WE# control signals. Further DMA channel 0 and IRQ2 are connected. Pin compatible FPGAs are EP1C6 and EP1C12. Configuration of the FPGA is done with a serial SPI-EEPROM by the FPGA itsself after RESET (serial master mode). This configuration needs about 40..60 ms (measured time between rising edge of PWRGOOD and rising edge of FPGA_CONF_DONE with preliminary logic without IP-cores, configuration time with IP-cores tbd) when data compression is used. Reprogramming needs either an ALTERA ByteBlaster II cable or can be done with a special update program directly fom the module.
One channel of the CAN controller needs 3232 LEs and 4352 memory bits for ALTERA (source BOSCH C_CAN IP module).
One channel of a UART with FIFO and IrDA needs 631 LEs and 1216 memory bits for ALTERA (source H16750 UART IP from CAST Inc.)
Two CAN channels and four UART channels means 8988 LEs and 13568 memory bits from 14 M4K blocks for ALTERA.
Adding the Compact Flash driver and the glue logic for audio etc. leads to a total utilization of about 150..200 LEs more.
So we have a total utilization of about 9100 LEs and 13600 memory bits for ALTERA.
4 UARTs, 2 CAN channels, CF will fit in an ALTERA EP1C12.
When reducing to 2 UARTs, 1 CAN, CF, audio control and PCI arbiter patch the design should fit in an ALTERA EP1C6.

6.3. CPLD

A CPLD ispMACH4064 is mounted including all necessary logic not realized in the FPGA. It will control an external quadruple UART, controls PENIRQ from touch control, emulate I2S and L3 ports for audio and generate clocks for audio, IrDA and the UARTs.

6.4. Power Supply

Input voltage for the developer board is 5VDC. The LCD board will be supplied by 12VDC from the same power supply (UMEC, 5V/3A, 12V/1A).
Power Estimation (worst case calculation):

Device	+5V [mA]	+3.3V [mA]	+1.5V [mA]
A9M9360 Module		400	
A9M9750 Module	300(*)	600	
FPGA ALTERA		200	900
CPLD Lattice ispMACH4064		50	
2 RS232 driver		50	
LCD		160	
USB	100		
CAN (2 channels)		50	
Touch		20	
Compact Flash		500	
Mini PCI		660	
Audio		50	
Sum with A9M9750 or A9M9360	100.. 400	700.. 2340	900

(*) 5V connected to VLIO only A9M9750_0 prototype modules without power sequencing
An ALTERA Cyclone FPGA EP1C12 needs +3.3V/200mA VCCIO and +1.5V/900mA VCCINT. +1.5V/900mA is generated by a switching regulator from 5V.

The 3.3V_IN is generated by a switching regulator TPS64200 with external FET and diode (3.3V@2A). We take the same circuit slightly modified for the generation of 1.5V/1A FPGA core voltage. 3.3V_IN is connected to the module; all peripherals on the board are powered with switched +3.3V and 3.3V_PCI from two power FET switches TPS2022 controlled by PWREN from the module. A pull up on PWREN switches default on. Usage of A9M9750_0 modules without power sequencing on the board need prior modification (VLIO connected to +5V for module without power sequencing; VLIO connected to 3.3V_IN for modules with power sequencing). A9M9750_1,2 and A9M9360 modules have power sequencing and run on this board without modification.

LEDs indicate power input 5V, 3.3V_IN, 3.3V, 3.3V_PCI and 1.5V onboard voltage at the developer board. Indicating 1.5V needs a comparator stage with 5V supply to ensure the minimum forward voltage of 1.6..2V of the LED. This stage is set to 1.35V threshold on the inverting input, so 1.5V will activate the LED.

3.3V_IN and 1.5V are supervised with U16. Failure asserts RSTIN#.

Power for the A9M9750 module is 3.3V_IN for I/O voltages and +3.3V_IN or +5V for VLIO used for the core voltage generation on the module. This guaranties for the module that its onboard core voltage will be the first to rise (important for all NetSilicon CPUs; ensures safe startup for prototypes and later generations). A9M9360 and A9M9750_1,2 have power sequencing on the module.

6.5. Debug LED

A green debug LED LE4 is connected with its cathode to ground. The anode has a 1K serial resistor and is wired via Jumper J13 to GPIO47 to allow universal usage on the board. Jumper open, if usage of GPIO47 other than driving LED.

6.6. 2 User Push Buttons

Two user push buttons S2,3 control GPIO45 and GPIO46. Buffers U1 decouple the signals which are slightly debounced. Optionally the FPGA status signals FPGA_STATUS1 (FPGA_CONF_DONE) and FPGA_STATUS2 (FPGA_STATUS#) are logically ANDed with the push buttons (signal active means then either push button or status active). This option needs two resistors mounted (R21,22). Due to the partial changed usage of the GPIOs with the A9M9630 module there are serial 1K resistors between the buffer and the GPIOs. This allows usage of the GPIOs as outputs too (important for A9M9360 module and USB PHY control with GPIO45).

6.7. RESET Control

A push button S1 allows manual RESET by pulling MAN_RST# at U16 to ground. U16 pulls RSTIN# to low. Signals RSTIN#, PWRGOOD and RSTOUT# are available on the 2.54mm extension connectors.

As the UART_RESET signal for the external UART is generated on the CPLD connected to RSTOUT#, reset sources on the module will reset the external UART (the UARTs in the FPGA will use RSTOUT# too).

6.8. JTAG Interfaces

The developer board has a 20-pin JTAG interface (X13) and an 8-pin JTAG-Booster connector (X12).

6.9. Configuration Switches

8 configuration switches S4 allow remote configuration of 4 hardware and 4 software configuration pins.

6.10. RS232 Interface

Additional quadruple UART (either made by the FPGA or additional ST16C754 chip) provides two RS232 Interfaces with driver and RS232 signals at DB9 connectors (channels 0, 1), further connected to 10 pin headers providing 3.3V signals (channels 0, 1, 2, 3). Channel 3 has an additional jumpers J5. It allow to connect RXD3 to an IrDA converter with an IrDA transceiver. The RS232 driver chips U4,5 support baud rates up to 230400 Bd. Types MAX3241 and MAX 3243 are allowed. They can be disabled by jumpers J2,3 to allow other usage of the signals from channel A and B via 10-pin header. Most signals of the serial communication resources on A9M9750/A9M9360 are used for other purposes and have some bugs in prototype NS9750 CPUs.

External UART clock (18.432MHz) is made with the CPLD. No delay at powerup after RESET is necessary to allow the CPLD to start. After this time the UART clock is available.

UART_RESET is made in the CPLD by inverting RSTOUT# from the module. A software UART RESET may be implemented in the CPLD.

6.11. IrDA Interface

RXD3 can be routed with jumper J5 to the IrDA converter U9. Setup and reset of this converter is done via RTS3# and DTR3#. The converter is connected to the IrDA transceiver V6 with the power stages, the Ir emitter LED and the receiver photo element.

6.12. SPI Interface

SPI channels A is used by the touch controller of the LCD and channel B is used by the audio channel. Channels C and D can be used, if no LCD is used with A9M9750 module or neither LCD nor USB PHY is used with the A9M9360 module. The signals for channel C and D are found on the expansion connectors X10,11 and on the LCD connector X25.

6.13. USB Interfaces

USB connectors for USB host (X14) and USB device (X15) are provided. USB is usable either in host or device mode, not both parallel with the A9M9750 module. Configuration with jumper field J4. Using the A9M9360 module allows parallel usage of USB host and device; USB device has an USB PHY MAX3454E U20 on the board controlled by 7 GPIOs from the module. This device channel can be selected by J4. The USB signals are 5V tolerant and they are ESD protected up to 15KV (human body model) by the chip.

The 22R series resistor are placed near the connectors. The signal USBH_DT/PW switches a 1k5 pull-up resistor to the USBD+ or USBD- line selecting low speed or full speed devices.

MAX890 supervises the current limit of a connected USB device. Threshold is set to 0.9A +/- 20%. Its FAULT# output is connected to the signal USBH_OVERCURR. FAULT# low signals either current limit or over temperature.

USB_INTPHY_P and USB_INTPHY_N pins of the NS9750 and NS9360 are not 5V tolerant, so a level limitation with shottky diodes V8..11 to Gnd and +3.3V is inserted between CPU signals and 22R serial resistors (current about 100mA @ 5V).

The USB_INTPHY signals from the module are connected with 0R resistors to the extension connectors allowing measurements. The stub can be removed when signal integrity problems occur.

6.14. CAN Interface

Planned as a future option, the FPGA U17 will emulate a 2 channel CAN controller. 2 driver chips U13,14 and two 10-pin headers X5,6 are mounted on the board. Every channel has a jumper (J11,12) for optional termination of the CAN lines. Transceivers are 3.3V types; no level translation is needed, CANL0,1 and CANH0,1 signals are 5V tolerant. As an option the drivers can be omitted to get the CANTX and CANRX signals (mounting option, drivers U13,14 not mounted, R99..102 mounted).

The reserved CANTX and CANRX signals from the module are routed to CAN channel 0. If using a module with CAN, the FPGA U17 has to be reprogrammed to disable CAN channel 0 in the FPGA.

6.15. Ethernet Interface

On the developer board an Ethernet connector X17 for 10/100MHz mode, with integrated transformer, activity/link and speed LEDs is provided. 100R series resistors limit LED current to about 7mA.

6.16. Compact Flash Interface

A 50 pin CompactFlash Card header Type 2 with ejector is provided (X29). It is placed at the bottom side of the PCB. Control and connection to memory bus is done with a FPGA. A logic device enables the access of the Compact Flash in 16bit mode.

Only 3.3V CompactFlash cards can be used.

6.17. Mini PCI Interface

A 124 pin Mini PCI Card header (Type III) with ejector is provided (X28). It is placed at the top side of the PCB.

Only 3.3V Mini PCI cards can be used; 5V power supply pins are not connected.

The signal PCICLK is defined with a length of 25.4mm ± 2.5mm on the MiniPCI card, instead of 63.5 mm on a standard PCI card.

The length of the PCI clock on the module A9M9750 is defined with 30mm (current length for 9750_0 is 25.2 mm, for 9750_1 is 14.8mm). The board to board connector on the A9M9750DEV is defined with 8mm.

To be able to connect a further PCI device to the expansion connectors an additional clock signal is routed to the expansion connectors. For calculating the resulting clock length, we assume, that it must be possible to connect an standard PCI slot via a small PCB to the expansion connector. We need to add following lengths:

Board-to-Board = 16mm (equal to PC/104 connector system)

Clock length on PCI card = 63.5mm

Trace length to connected expansion connector with PCI slot = 30 mm.

Signal IDSEL on the header is connected via 50R resistor to PCI_AD16 (PCI device 5) PCI_IDSEL from module in host mode has to be connected to PCI_AD11 (PCI device 0). This is done on the A9M9750_1 modules, optional on the dev board possible.

The PCI interface is unused and not connected on the A9M9360 module (NS9360 CPU is without PCI).

6.18. PCI Arbiter Patch, Timing Calculations and Realisation

A bug in the PCI arbiter grants mastership to a bus master still, when he negates REQ# and IRDY# in the same clock cycle, if no other master is requesting the bus. After 16 clock cycles this master is considered “broken” by the arbiter due to not taking over mastership again and sets a bit in the PCI arbiter status register ignoring all further bus requests by this master (see “appnote_pciarbiter.pdf” from Netsilicon published in 2004).

Besides a software workaround a 1-bit state machine realised in hardware will negate the REQ# signal when the master takes control of the bus preventing for the NS9750 to see REQ# active with negated IRDY#. This workaround needs a timing described below to work.

Signals involved are PCI_CLK, PCI_FRAME#, PCI_RST#, PCI_GNT0#, PCI_GNT1#, PCI_GNT2#, PCI_GNT3#, SPCI_REQ0#, SPCI_REQ1#, SPCI_REQ2#, SPCI_REQ3#, PCI_IRDY# generating the gated PCI_REQ0#, PCI_REQ1#, PCI_REQ2#, PCI_REQ3# for the NS9750.

PCI cycle time is 30ns @ 33.333MHz minimum, so PCI_REQ1# has to be valid latest after 30ns to get sampled by the arbiter.

The hardware workaround has a maximum of three stage delays routed in a programmable logic chip. Another 11ns delay has to added before PCI_FRAME# gets valid after PCI_CLK valid, so the resulting time margin is reduced to 19ns. Taking a worts case realisation in a CPLD or FPGA with three stages, we need delay times of less than 6.5ns per stage in the logic chip.

The CPLD MACH4064-10 has a worst case delay time of 10ns per stage, too slow to be safe.

The FPGA EP1C6/12 in the slowest version (-8) has a worst case delay time of 4.9ns per stage resulting in a worst case delay of 15ns, sufficient for the planned workaround.

This workaround is prepared on A9M9750DEV_1 for PCI channel1 only. Signals PCI_CLK_SLOT, PCI_FRAME#, PCI_RESET#, PCI_GNT1#, PCI_IRDY#, SPCI_REQ1# and PCI_REQ1# are connected to the FPGA U17. Default a logic without hardware workaround is assumed with bypass resistor R140 populated. If an FPGA logic version supports the hardware workaround, these resistors must be depopulated. before using this version.

A9M9750DEV_2 has PCI channels 0..3 prepared. Signals PCI_CLK_SLOT, PCI_FRAME#, PCI_RESET#, PCI_IRDY#, PCI_GNT0#, PCI_GNT1#, PCI_GNT2#, PCI_GNT3#, SPCI_REQ0#, SPCI_REQ1#, SPCI_REQ2#, SPCI_REQ3#, PCI_REQ0#, PCI_REQ1#, PCI_REQ2#, and PCI_REQ3# are connected to the FPGA U17. Default the bypass resistors R139 (ch0), R140 (ch1), R141 (ch2) and R142 (ch3) are populated. If an FPGA logic version supports the hardware workaround, these resistors must be depopulated. before using this version.

6.19. LCD Interface

The Sharp LQ57Q3DC02 TFT display is supported. It has a colour resolution of 18bpp. 18bpp are supported by the A9M9750 and A9M9360 module. An additional pcb (LCDMODARM) is used, which includes the power connector, backlight module, LCD connector and touch interface connector with a touch controller connected to A9M9750 or A9M9360 via SPI channel A. The signal lines from LCD and touch to the developer board are connected by a 40pin flat ribbon cable connected to X25. 22R series resistors are provided at the CLK lines. The configuration signals R/L (horizontal direction), U/D (vertical direction) and V/Q (using VGA or quarter VGA signals) are not equipped (normally set on the LCD).

6.20. Touch Screen

Control of touch screen via SPI channel A from A9M9750 / A9M9360 and via FPGA or CPLD to IRQ2 routed PENIRQ#. The touch controller is mounted on the LCDMODARM board. Connection with a 10 pole flat-cable connected to X27.

6.21. Audio Codec

The UDA1341TS is used as audio codec. It is connected to an emulated IIS-interface of the A9M9750 and A9M9360 needing SPI B, some logic in the FPGA and some GPIOs. Connectors for speaker or line-out (X22), microphone (X23) and line-in (X24) are provided at the developer board.
The audio codec will communicate with the A9M9750 module through an SPI serial interface. The SPI serial channel B of the A9M9750 and the SPI serial channel of the UDA1341 are configured in slave mode. The FPGA or the CPLD is the master of the SPI channel, that means that the FPGA or CPLD must generate the SPI_CLK and the SPI_SEL# signals.

The audio channel on board can be configured to have four different audio qualities; CD, FM, FM2 and Phone. The different audio qualities are controlled with two bits; AUDIO_QUAL(1) and AUDIO_QUAL(0). Next table shows the different audio qualities and the clocks associated to them:

AUDIO_QUAL(1)	AUDIO_QUAL(0)	QUALITY	SAMPLE RATE	BITS	MODE	SPI_CLK	AUDIO_CLK
0	0	CD	44,1 KHz	16	Stereo	1,4112 MHz	11,2896 MHz
0	1	FM	22,05 KHz	16	Stereo	705,6 KHz	11,2896 MHz
1	0	FM2	16 KHz	16	Stereo	512 KHz	4,096 MHz
1	1	Phone	8 KHz	8	Stereo	128 KHz	4,096 MHz

Some features of the audio codec will be selected through an L3 interface. This interface will be controlled with L3_CLK and L3_DAT from FPGA or CPLD and with the signal L3_MODE generated by software using GPIO4 from the A9M9750 /A9M9360 module.
The UDA1341TS audio codec provides two audio inputs and one audio output. Two audio input interfaces will be mounted on the developers board; one for a “Line-In” input and a second one for a microphone input. One audio output interface will be mounted on the board; it is usable for “Line-out” output or headphone output.

6.22. Extension Connectors

Extension connectors X3,4 are provided to support also the extended version of the A9M9750 module. The signals are connected to the corresponding expansion connectors. The signals have to be defined.

6.23. Expansion Connectors

The board provides expansion connectors X10, X11, X20, X21, X30, X31, X40, X41, which can be used to plug onto a customized board. Most of the signals from the module are connected to these expansion connectors.

7. CPU Port Usage A9M Modules

7.1. Module A9M9750

Port	Usage, Direction	Comment
GPIO0	SPIB_DO, OUT	SPI audio
GPIO1	SPIB_DI, IN	SPI audio
GPIO2	GPIO2, unused	free
GPIO3	DMA0_REQ, IN	DMA0 FPGA or CPLD
GPIO4	GPIO4, OUT	L3_MODE audio
GPIO5	DMA0_ACK, OUT	DMA0 FPGA or CPLD
GPIO6	SPIB_CLK, IN	SPI audio in slave mode
GPIO7	SPIB_CE#, IN	SPI audio in slave mode
GPIO8	SPIA_DO, OUT	SPI touch
GPIO9	SPIA_DI, IN	SPI touch
GPIO10	GPIO10, unused	free
GPIO11	IRQ2 dupe, IN	INT from FPGA or CPLD
GPIO12	FPGA_CS0#, OUT	CS# FPGA Configuration EEPROM via MUX U41
GPIO13	IRQ0 dupe, IN	used for RTC_INT# on module
GPIO14	SPIA_CLK, OUT	SPI touch
GPIO15	SPIA_EN#, OUT	SPI touch
GPIO16	USB_OVERCURRENT, IN	USB
GPIO17	USB_DT/PWR, OUT	USB
GPIO18	LCD_PWR_EN, OUT	LCD
GPIO19	LCD_HSYNC, OUT	LCD
GPIO20	LCD_CLK, OUT	LCD
GPIO21	LCD_VFSYNC, OUT	LCD
GPIO22	LCD_BIAS_D_EN, OUT	LCD
GPIO23	LCD_LINE_END, OUT	LCD
GPIO24	LCD_D0, I/O	LCD
GPIO25	LCD_D1, I/O	LCD
GPIO26	LCD_D2, I/O	LCD
GPIO27	LCD_D3, I/O	LCD
GPIO28	LCD_D4, I/O	LCD
GPIO29	LCD_D5, I/O	LCD
GPIO30	LCD_D6, I/O	LCD
GPIO31	LCD_D7, I/O	LCD
GPIO32	LCD_D8, I/O	LCD
GPIO33	LCD_D9, I/O	LCD
GPIO34	LCD_D10, I/O	LCD
GPIO35	LCD_D11, I/O	LCD
GPIO36	LCD_D12, I/O	LCD
GPIO37	LCD_D13, I/O	LCD
GPIO38	LCD_D14, I/O	LCD
GPIO39	LCD_D15, I/O	LCD
GPIO40	LCD_D16, I/O	LCD
GPIO41	LCD_D17, I/O	LCD
GPIO42	FPGA_DCLK, OUT	CLK FPGA Config. EEPROM via MUX U41
GPIO43	FPGA_DATA0, IN	DO FPGA Config. EEPROM via MUX U41
GPIO44	FPGA_ASDO, OUT	DI FPGA Config. EEPROM via MUX U41
GPIO45	Push button 1, IN	User push button 1 (& FPGA_CONF_DONE opt.)
GPIO46	Push button 2, IN	User push button 2 (& FPGA_STATUS# opt.)
GPIO47	debug LED, OUT	Debug LED
GPIO48	GPIO48, unused	free
GPIO49	R/B# NAND Flash, IN	n.a., usage on module

7.2. Module A9M9360

Port	Usage, Direction	Comment
GPIO0	SPIB_DO, OUT	SPI audio
GPIO1	SPIB_DI, IN	SPI audio
GPIO2	GPIO2, unused	free
GPIO3	DMA0_REQ, IN	DMA0 FPGA or CPLD
GPIO4	GPIO4, OUT	L3_MODE audio
GPIO5	DMA0_ACK, OUT	DMA0 FPGA or CPLD
GPIO6	SPIB_CLK, IN	SPI audio in slave mode
GPIO7	SPIB_CE#, IN	SPI audio in slave mode
GPIO8	SPIA_DO, OUT	SPI touch
GPIO9	SPIA_DI, IN	SPI touch
GPIO10	GPIO10, unused	free
GPIO11	IRQ2 dupe, IN	INT from FPGA or CPLD
GPIO12	FPGA_CS0#, OUT	CS# FPGA Configuration EEPROM via MUX U41
GPIO13	IRQ0 dupe, IN	used for RTC_INT# on module
GPIO14	SPIA_CLK, OUT	SPI touch
GPIO15	SPIA_EN#, OUT	SPI touch
GPIO16	USB_OVERCURRENT, IN	USB
GPIO17	USB_DT/PWR, OUT	USB
GPIO18	LCD_PWR_EN, OUT	LCD
GPIO19	LCD_HSYNC, OUT	LCD
GPIO20	LCD_CLK, OUT	LCD
GPIO21	LCD_VFSYNC, OUT	LCD
GPIO22	LCD_BIAS_D_EN, OUT	LCD
GPIO23	LCD_LINE_END, OUT	LCD
GPIO24	LCD_D0, I/O	LCD
GPIO25	LCD_D1, I/O	LCD
GPIO26	LCD_D2, I/O	LCD
GPIO27	LCD_D3, I/O	LCD
GPIO28	LCD_D4, I/O	LCD
GPIO29	LCD_D5, I/O	LCD
GPIO30	LCD_D6, I/O	LCD
GPIO31	LCD_D7, I/O	LCD
GPIO32	LCD_D8, I/O	LCD
GPIO33	LCD_D9, I/O	LCD
GPIO34	LCD_D10, I/O	LCD
GPIO35	LCD_D11, I/O	LCD
GPIO36	LCD_D12, I/O	LCD
GPIO37	LCD_D13, I/O	LCD
GPIO38	LCD_D14, I/O	LCD
GPIO39	LCD_D15, I/O	LCD
GPIO40	LCD_D16, I/O	LCD
GPIO41	LCD_D17, I/O	LCD
GPIO42	FPGA_DCLK, OUT or USB_PHY_D+, bid	FPGA_DCLK Config. EEPROM or USB device data+ to external USB PHY via MUX U41
GPIO43	FPGA_DATA0, IN or USB_PHY_D-, bid	FPGA_DATA0 out Config. EEPROM or USB device data- to external USB PHY via MUX U41
GPIO44	FPGA_ASDO, OUT or USB_PHY_OE#, OUT	FPGA_ASDO in Config. EEPROM or USB device output enable to external USB PHY via MUX U41
GPIO45	Push button 1, IN or USB_PHY_RXD, OUT	User push button 1 (AND FPGA_CONF_DONE optional) or USB device phy rx data function via MUX U40

GPIO46	Push button 2, IN	User push button 2 (AND FPGA_STATUS# opt.)
GPIO47	debug LED, OUT	Debug LED
GPIO48	GPIO48, unused, or USB_PHY_SUSP, OUT	free or USB external PHY device suspend control via MUX U40
GPIO49	R/B# NAND Flash, IN	n.a., usage on module for NAND Flash
GPIO50	used on module for MII_MDIO	GPIO n.a., usage on module for ethernet PHY
GPIO51	used on module for MII_RXDV	GPIO n.a., usage on module for ethernet PHY
GPIO52	used on module for MII_RXER	GPIO n.a., usage on module for ethernet PHY
GPIO53	used on module for MII_RXD0	GPIO n.a., usage on module for ethernet PHY
GPIO54	used on module for MII_RXD1	GPIO n.a., usage on module for ethernet PHY
GPIO55	used on module for MII_RXD2	GPIO n.a., usage on module for ethernet PHY
GPIO56	used on module for MII_RXD3	GPIO n.a., usage on module for ethernet PHY
GPIO57	used on module for MII_TXEN	GPIO n.a., usage on module for ethernet PHY
GPIO58	used on module for MII_TXER	GPIO n.a., usage on module for ethernet PHY
GPIO59	used on module for MII_TXD0	GPIO n.a., usage on module for ethernet PHY
GPIO60	used on module for MII_TXD1	GPIO n.a., usage on module for ethernet PHY
GPIO61	used on module for MII_TXD2	GPIO n.a., usage on module for ethernet PHY
GPIO62	used on module for MII_TXD3	GPIO n.a., usage on module for ethernet PHY
GPIO63	used on module for MII_COL	GPIO n.a., usage on module for ethernet PHY
GPIO64	used on module for MII_CRS	GPIO n.a., usage on module for ethernet PHY
GPIO65	used on module for MII_MDINT#	GPIO n.a., usage on module for ethernet PHY
GPIO66	A22, OUT	A22 to FPGA
GPIO67	A23, OUT	A23 to FPGA
GPIO68	A24, OUT	A24 to FPGA
GPIO69	A25, OUT	A25 to FPGA
GPIO70	I2C_SCL	I2C, A26 lost
GPIO71	I2C_SDA	I2C, A27 lost
GPIO72	WAIT#	routed as WAIT# to FPGA or CPLD

8. Usage and Pinning of ALTERA FPGA

Planned is the implementation of several stages:

1. A9M9750 / 9360 32-bit data, 26-bit address interface. Control signals are EXT_CS0#, EXT_CS2#, EXT_CS3#, WAIT#, OE#, WE#, DMA0REQ and DMA0ACK, IRQ2, EXT_BE0..3 and RSTOUT#.

2. Optional glue logic for emulation of I2S and L3 bus with SPIB and GPIO of the module using the signals L3MODE, SPIB_SEL#, SPIB_CLK, AUDIO_CLK, AUD_L3_SDA, AUD_L3_SCL (normally in CPLD realised)

3. Compact Flash with 16-bit CF_data, 10-bit CF_address and control signals CF_CD1#, CF_CE1,2#, CF_OE#, CF_WP/IOIS16#, CF_IORD#, CF_IOWR#, CF_WE#, CF_RDY/IRQ#, CF_RESET, CF_WAIT#, CF_REG#.

4. PCI arbiter patch for NS9750 CPU. Needs PCI_CLK_SLOT, PCI_FRAME#, PCI_RESET#, PCI_GNT0..3#, SPCI_REQ0..3# and PCI_IRDY# signals to generate PCI_REQ0..3# signals with right timing

5. Up to four UARTs UART0..3 with all modem signals (TXD, RXD, RTS#, CTS#, DSR#, DTR#, DCD# and RI#).

6. Up to two CAN channels for CAN protocol version 2.0A, B with CANTX0,1 and CANRX0,1.

Either an ALTERA Cyclone EP1C6 with 5980 Logic Elements (LEs) and 20 M4K blocks RAM or an EP1C12 with 12060 LEs and 52 M4K block RAM are used. Both FPGAs have a 256 pin FBGA case. They are pin compatible. The smaller chip will drive only one CAN and less UART channels.

If modules with own CAN controller are used, The logic of the FPGA has to be reprogrammed to disable the channel 0 CAN controller.

8.1. Configuration FPGA

ALTERA Cyclone EP1C6 needs 145.902 byte and EP1C12 needs 290.816 byte for configuration. We will use a serial configuration EEPROM from Altera EPCS4 with 4Mbits. The FPGA will run in active serial (AS) mode. Clock and control will come from the FPGA. Signals used from FPGA: CONFIG#, DATA0, DCLK, CONF_DONE and STATUS#. Signals used from serial EEPROM: DATA, DCLK, CS#, ASDI. A 10-pin header X9 allows connection of an ALTERA ByteBlaster II download cable to reprogram the EEPROM. GPIO12,42,43,44 are connected to the 4 EEPROM lines too with quadruple analog switch U41. Mode selection with J16,17. This allows remote programming from the module with a special program or via JTAG. FGPA is disabled by shorting pins 4-6 on X9.

8.2. Clock Concept FPGA

The FPGA contains two independant PLLs with input frequency prescaler (1..32), VCO multiplier (1..32) and independant output divider (1..32) for three channels (2 internal, one pin). The VCOs have to run with a frequency between 500 and 1000MHz.

A 33.333MHz clock generator is connected to PLL1. Multiplied with 24 a 800MHz VCO clock is the result. A 36.864MHz clock generator is connected to PLL2. Multiplied with 18 the VCO clock is 663,552MHz.

Different clocks are needed for the multiple stages in the FPGA and on the board:

1. 50MHz as internal clock for th FPGA glue logic. Made from PLL1 by division by 16.

2. 11.2896MHz for the fast audio clock. Provided by external generator.

3. 25MHz for the CAN channels. Made from PLL1 with division by 32.

4. 18.432MHz for the internal UARTs. Made from PLL2 with division by 18 and further division by 2.

8.3. PCI Arbiter Patches

A bug in the PCI arbiter grants mastership to a bus master still, when he negates REQ# and IRDY# in the same clock cycle, if no other master is requesting the bus. After 16 clock cycles this master is considered “broken” by the arbiter due to not taking over mastership again and sets a bit in the PCI arbiter status register ignoring all further bus requests by this master (see “appnote_pciarbiter.pdf” from Netsilicon published in 2004).

Besides a software workaround a 1-bit state machine realised in hardware will negate the REQ# signal when the master takes control of the bus preventing for the NS9750 to see REQ# active with negated IRDY#. This workaround needs a timing described below to work.

Signals involved are PCI_CLK, PCI_FRAME#, PCI_RST#, PCI_GNT1#, PCI_GNT2#, PCI_GNT3#, SPCI_REQ1#, SPCI_REQ2#, SPCI_REQ3#, PCI_IRDY# generating the gated PCI_REQ1#, PCI_REQ2#, PCI_REQ3# for the NS9750.

(future extension in A9M9750DEV_2, A9M9750DEV_1 has only SPCI_REQ1# and PCI_REQ1# connected)

SPCI_REQ1# is connected to the mini-PCI slot, SPCI_REQ2,3# to the extension pins X20,21.

PCI_REQ1..3# is connected to the module connector x2

SPCI_REQ1..3# can be connected to PCI_REQ1..3# with a 0R resistor to bypass the PCI patch in the FPGA for every channel.

8.4. Usage Bank 1

Bank	EP1C6, EP1C12 Pin Name	FBGA256 Pin Number	Type	Usage on developer board	comment
1	IO0_1/INIT_DONE	D4	IO	D0	not used for Conf
1	IO1_1/LVDS23n	C3	IO	D1	Data Bus Module
1	IO2_1/CLKUSR	C2	IO	D2	not used for Conf
1	IO3_1/LVDS22n	B1	IO	D3	
1	IO4_1/VREF0B1	G5	IO	D4	
1	IO5_1	F4	IO	D5	
1	IO6_1/LVDS21p	D3	IO	D6	
1	IO7_1/LVDS21n	E4	IO	D7	
1	IO8_1/DPCLK1	F5	IO	D8	
1	IO9_1/LVDS20p	E3	IO	D9	
1	IO10_1/LVDS20n	D2	IO	D10	
1	IO11_1/LVDS19p	E2	IO	D11	
1	IO12_1/LVDS19n	D1	IO	D12	
1	IO13_1/LVDS18p	F3	IO	D13	
1	IO14_1/LVDS18n	G3	IO	D14	

1	IO15_1/LVDS17p	F2	IO	D15	
1	IO16_1/LVDS17n	E1	IO	D16	
1	IO17_1/LVDS16p	G2	IO	D17	
1	IO18_1/LVDS16n	F1	IO	D18	
1	IO19_1/VREF1B1	H5	IO	D19	
1	IO20_1/CSO#	G4	CONF	FPGA_CS0#	to serial Conf EEPR
1	DATA0	H2	CONF	FPGA_DATA0	to serial Conf EEPR
1	CONFIG#	H3	CONF	FPGA_CONFIG#	to PWRGOOD w 1K
1	VCCA_PLL1	H6	PWR	+1.5V analog	PLL1 power
1	CLK0/LVDSCLK1p	G1	CLK	33.333MHz for PLL1	system, CAN
1	CLK1/LVDSCLK1n	H1	CLK	BCLKOUT	reserved for clk out
1	GNDA_PLL1	J6	PWR	AGnd	PLL1 Ground
1	GND_GPLL1	J5	PWR	AGnd	PLL1 Guard Ring
1	CEO#	H4	CONF	**pad for access**	cascading output
1	CE#	J4	CONF	FPGA_CE#	to Gnd via 4K7
1	MSEL0	J3	CONF	MSEL0	AS mode = Gnd
1	MSEL1	J2	CONF	MSEL1	AS mode = Gnd
1	DCLK	K4	CONF	FPGA_DCLK	to CLK EEPROM
1	IO21_1/ASDO	K3	CONF	FPGA_ASDO	to ASDI EEPROM
1	IO22_1/PLL1_OUTp	J1	IO	**pad for access**	MP25, free
1	IO23_1/PLL1_OUTn	K2	IO	D20	
1	IO24_1/LVDS7n	L3	IO	D21	
1	IO25_1/LVDS6p	K1	IO	D22	
1	IO26_1/LVDS6n	L1	IO	D23	
1	IO27_1/LVDS5p	L2	IO	D24	
1	IO28_1/LVDS5n	M1	IO	D25	
1	IO29_1/LVDS4p	N1	IO	D26	
1	IO30_1/LVDS4n	M2	IO	D27	
1	IO31_1/LVDS3p	N2	IO	D28	
1	IO32_1/LVDS3n	M3	IO	D29	
1	IO33_1/DPCLK0	L5	IO	D30	
1	IO34_1/LVDS2p	M4	IO	D31	
1	IO35_1/LVDS2n	N3	O	SPIB_SEL#	audio channel
1	IO36_1/VREF2B1	K5	O	AUDIO_CLK	fast and slow out
1	IO37_1	L4	I	11.2896MHz Input	fast audio clock in
1	IO38_1/LVDS1p	R1	O	SPIB_CLK	audio channel
1	IO39_1/LVDS1n	P2	IO	AUD_WS	Wire Patch (_1), connected in _2
1	IO40_1/LVDS0p	P3	IO	**Pad for access**	MP27, free
1	IO41_1/LVDS0n	N4	IO	**Pad for access**	MP5, free

8.5. Usage Bank 2

Bank	EP1C6, EP1C12 Pin Name	FBGA256 Pin Number	Type	Usage on developer board	comment
2	IO0_2/LVDS50n	B15	I	A0	Address bus module
2	IO1_2/LVDS50p	A15	I	A1	
2	IO2_2/LVDS49n	B14	I	A2	
2	IO3_2/LVDS49p	C13	I	A3	
2	IO4_2/LVDS48n	B13	I	A4	
2	IO5_2/LVDS48p	A13	I	A5	
2	IO6_2/LVDS47n	B12	I	A6	
2	IO7_2/LVDS47p	C12	I	A7	
2	IO8_2/DPCLK3	E12	I	A8	

2	IO9_2/VREF0B2	E11	I	A9	
2	IO10_2	E9	I	A10	
2	IO11_2/LVDS46n	D12	I	A11	
2	IO12_2/LVDS46p	D11	I	A12	
2	IO13_2/LVDS43n	C11	I	A13	
2	IO14_2/LVDS43p	B11	I	A14	
2	IO15_2/LVDS42n	A11	I	A15	
2	IO16_2/LVDS42p	B10	I	A16	
2	IO17_2/LVDS41n	C10	I	A17	
2	IO18_2/LVDS41p	D10	I	A18	
2	IO19_2/LVDS40n	A9	I	A19	
2	IO20_2/LVDS40p	B9	I	A20	
2	IO21_2/LVDS39n	D9	I	A21	
2	IO22_2/LVDS39p	C9	I	A22	
2	IO23_2/VREF1B2	E10	I	A23	
2	IO24_2/LVDS36n	C8	I	A24	
2	IO25_2/LVDS36p	D8	I	A25	
2	IO26_2/LVDS34p	E8	I	PCI_CLK_SLOT	PCI arbiter patch
2	IO27_2/LVDS33n	A8	I	PCI_FRAME#	PCI arbiter patch
2	IO28_2/LVDS33p	B8	O	3.6864MHz	to IrDA Converter
2	IO29_2/LVDS32n	D7	I	PCI_RESET#	PCI arbiter patch
2	IO30_2/LVDS32p	C7	I	PCI_GNT1#	PCI arbiter patch
2	IO31_2/LVDS31n	B7	I	PCI_IRDY#	PCI arbiter patch
2	IO32_2/LVDS31p	A6	I	SPCI_REQ1#	PCI arbiter patch
2	IO33_2/LVDS30p	E7	O	WAIT#	Ctrl Sign Module
2	IO34_2/LVDS29n	B6	I	EXT_OE#	
2	IO35_2/LVDS29p	C6	I	WE#	
2	IO36_2/LVDS28n	D6	O	DMA0_REQ	
2	IO37_2/LVDS28p	D5	I	DMA0_ACK	
2	IO38_2/VREF2B2	E6	O	AUD_L3_SCL	audio L3 port
2	IO39_2/DPCLK2	E5	IO	AUD_L3-SDA	audio L3 port
2	IO40_2/LVDS27n	C5	O	IRQ2	Interrupts to module
2	IO41_2/LVDS27p	B5	I	RSTOUT#	End boot from module
2	IO42_2/LVDS26n	A4	I	EXT_CS0#	
2	IO43_2/LVDS26p	B4	I	EXT_CS2#	
2	IO44_2/LVDS25n	C4	I	EXT_CS3#	
2	IO45_2/LVDS25p	B3	I	EXT_BE0#	
2	IO46_2/LVDS24n/DEV_OE	A2	I	EXT_BE1#	
2	IO47_2/LVDS24p/DEV_CLR#	B2	I	EXT_BE2#	

8.6. Usage Bank 3

Bank	EP1C6, EP1C12 Pin Name	FBGA256 Pin Number	Type	Usage on developer board	comment
3	IO0_3/LVDS75n	N13	I	EXT_BE3#	
3	IO1_3/LVDS75p	P14	IO	PCI_REQ2#	PCI arbiter patch (_2)
3	IO2_3/LVDS74n	P15	IO	PCI_REQ3#	PCI arbiter patch (_2)
3	IO3_3/LVDS74p	R16	IO	PCI_REQ0#	PCI arbiter patch (_2)
3	IO4_3/LVDS73n	N15	O	PCI_REQ1#	PCI arbiter patch
3	IO5_3/LVDS73p	N16	IO	CF_D0	Data Comp Flash
3	IO6_3/VREF2B3	K12	IO	CF_D1	
3	IO7_3	K14	IO	CF_D2	
3	IO8_3/DPCLK5	L12	IO	CF_D3	
3	IO9_3/LVDS72n	N14	IO	CF_D4	
3	IO10_3/LVDS72p	M13	IO	CF_D5	

3	IO11_3/LVDS71n	M14	IO	CF_D6	
3	IO12_3/LVDS71p	L13	IO	CF_D7	
3	IO13_3/LVDS70n	M15	IO	CF_D8	
3	IO14_3/LVDS70p	M16	IO	CF_D9	
3	IO15_3/LVDS69n	L14	IO	CF_D10	
3	IO16_3/LVDS69p	L15	IO	CF_D11	
3	IO17_3/LVDS68n	L16	IO	CF_D12	
3	IO18_3/LVDS68p	K16	IO	CF_D13	
3	IO19_3/PLL2_OUTn	K15	IO	CF_D14	
3	IO20_3/PLL2_OUTp	J16	IO	CF_D15	
3	CONF_DONE	K13	CONF	FPGA_STAT1	End config
3	STATUS#	J13	CONF	FPGA_STAT2	Status FPGA
3	TCK	J14	CONF	**pad for access**	JTAG
3	TMS	J15	CONF	**pad for access**	JTAG
3	TDO	H15	CONF	**pad for access**	JTAG
3	GNDG_PLL2	J12	PWR	to AGnd	Guard PLL2
3	GNDA_PLL2	J11	PWR	to AGnd	Gnd PLL2
3	CLK2/LVDSCLK2n	H16	CLK	**pad for access**	MP13, free
3	CLK3/LVDSCLK2p	G16	CLK	36.864MHz Input	for UARTs, Audio
3	VCCA_PLL2	H11	PWR	+1.5V analog	Power PLL2
3	TDI	H14	CONF	**pad for access**	JTAG
3	IO21_3/VREF1B3	H12	IO	PCI_GNT0#	PCI Patch
3	IO22_3/LVDS59n	G14	O	CF_A0	Addr Comp Flash
3	IO23_3/LVDS59p	G13	O	CF_A1	
3	IO24_3/LVDS58n	G15	O	CF_A2	
3	IO25_3/LVDS58p	F16	O	CF_A3	
3	IO26_3/LVDS57n	F14	O	CF_A4	
3	IO27_3/LVDS57p	F13	O	CF_A5	
3	IO28_3/LVDS56n	F15	O	CF_A6	
3	IO29_3/LVDS56p	E16	O	CF_A7	
3	IO30_3/LVDS55n	E15	O	CF_A8	
3	IO31_3/LVDS55p	D16	O	CF_A9	
3	IO32_3/LVDS54n	D15	O	CF_A10	
3	IO33_3/LVDS54p	E14	IO	PCI_GNT2#	PCI Patch (_2)
3	IO34_3/DPCLK4	F12	IO	PCI_GNT3#	PCI Patch (_2)
3	IO35_3/LVDS53n	E13	IO	SPCI_REQ2#	PCI Patch (_2)
3	IO36_3/LVDS53p	D14	IO	SPCI_REQ3#	PCI Patch (_2)
3	IO37_3	H13	IO	SPCI_REQ0#	PCI Patch (_2)
3	IO38_3/VREF0B3	G12	I	CF_CD1#	Ctrl Comp Flash
3	IO39_3/LVDS52n	B16	O	CF_CE1#	
3	IO40_3/LVDS52p	C15	O	CF_CE2#	
3	IO41_3/LVDS51n	C14	O	CF_OE#	
3	IO42_3/LVDS51p	D13	IO	CF_WP/IOIS16#	

8.7. Usage Bank 4

Bank	EP1C6, EP1C12 Pin Name	FBGA256 Pin Number	Type	Usage on developer board	comment
4	IO0_4/LVDS102p	R2	O	CF_IORD#	Ctrl Comp Flash
4	IO1_4/LVDS102n	T2	O	CF_IOWR#	
4	IO2_4/LVDS101p	R3	O	CF_WE#	
4	IO3_4/LVDS101n	P4	I	CF_RDY/IRQ#	
4	IO4_4/LVDS100p	R4	O	CF_RESET	
4	IO5_4/LVDS100n	T4	I	CF_WAIT#	

4	IO6_4/LVDS99p	R5	O	CF_REG#	
4	IO7_4/LVDS99n	P5	I	PENIRQ#	Interrupt Touch
4	IO8_4/DPCLK7	M5	IO	**pad for access**	MP14, free
4	IO9_4/VREF2B4	M6	IO	**pad for acess**	MP15, free
4	IO10_4/LVDS98p	N5	O	CANTX0	CAN0
4	IO11_4/LVDS98n	N6	I	CANRX0	
4	IO12_4/LVDS97p	P6	O	CANTX1	CAN1
4	IO13_4/LVDS97n	R6	I	CANRX1	
4	IO14_4/LVDS96p	M7	O	TXD0	UART0
4	IO15_4/LVDS95p	T6	I	RXD0	
4	IO16_4/LVDS95n	R7	O	RTS0#	
4	IO17_4/LVDS94p	P7	I	CTS0#	
4	IO18_4/LVDS94n	N7	I	DSR0#	
4	IO19_4/LVDS93p	R8	O	DTR0#	
4	IO20_4/LVDS93n	T8	I	DCD0#	
4	IO21_4/LVDS92p	M8	I	RI0#	
4	IO22_4/LVDS90p	N8	O	TXD1	UART1
4	IO23_4/LVDS90n	P8	I	RXD1	
4	IO24_4/VREF1B4	M10	O	RTS1#	
4	IO25_4/LVDS87p	R9	I	CTS1#	
4	IO26_4/LVDS87n	T9	I	DSR1#	
4	IO27_4/LVDS86p	P9	O	DTR1#	
4	IO28_4/LVDS86n	N9	I	DCD1#	
4	IO29_4/LVDS85p	R10	I	RI1#	
4	IO30_4/LVDS85n	T11	IO	**pad for acess**	MP16, free
4	IO31_4/LVDS84p	N10	IO	**pad for acess**	MP17, free
4	IO32_4/LVDS84n	P10	O	TXD2	UART2
4	IO33_4/LVDS83p	R11	I	RXD2	
4	IO34_4/LVDS83n	P11	O	RTS2#	
4	IO35_4/LVDS80p	N11	I	CTS2#	
4	IO36_4/LVDS80n	N12	I	DSR2#	
4	IO37_4	M9	O	DTR2#	
4	IO38_4/VREF0B4	M11	I	DCD2#	
4	IO39_4/DPCLK6	M12	I	RI2#	
4	IO40_4/LVDS79p	P12	O	TXD3	UART3
4	IO41_4/LVDS79n	R12	I	RXD3	
4	IO42_4/LVDS78p	T13	O	RTS3#	
4	IO43_4/LVDS78n	R13	I	CTS3#	
4	IO44_4/LVDS77p	R14	I	DSR3#	
4	IO45_4/LVDS77n	P13	O	DTR3#	
4	IO46_4/LVDS76p	T15	I	DCD3#	
4	IO47_4/LVDS76n	R15	I	RI3#	

8.8. Power, Ground

Bank	EP1C6, EP1C12 Pin Name	FBGA256 Pin Number	Type	Usage on developer board	comment
	VCCINT	A7	PWR	+1.5V	Core voltage
	VCCINT	A10	PWR	+1.5V	Core voltage
	VCCINT	G8	PWR	+1.5V	Core voltage
	VCCINT	G10	PWR	+1.5V	Core voltage
	VCCINT	H7	PWR	+1.5V	Core voltage
	VCCINT	H9	PWR	+1.5V	Core voltage
	VCCINT	J8	PWR	+1.5V	Core voltage

	VCCINT	J10	PWR	+1.5V	Core voltage
	VCCINT	K7	PWR	+1.5V	Core voltage
	VCCINT	K9	PWR	+1.5V	Core voltage
	VCCINT	T7	PWR	+1.5V	Core voltage
	VCCINT	T10	PWR	+1.5V	Core voltage
	VCCIO1	C1	PWR	+3.3V	IO voltage bank 1
	VCCIO1	G6	PWR	+3.3V	IO voltage bank 1
	VCCIO1	P1	PWR	+3.3V	IO voltage bank 1
	VCCIO2	A14	PWR	+3.3V	IO voltage bank 2
	VCCIO2	F10	PWR	+3.3V	IO voltage bank 2
	VCCIO2	F7	PWR	+3.3V	IO voltage bank 2
	VCCIO2	A3	PWR	+3.3V	IO voltage bank 2
	VCCIO3	P16	PWR	+3.3V	IO voltage bank 3
	VCCIO3	K11	PWR	+3.3V	IO voltage bank 3
	VCCIO3	C16	PWR	+3.3V	IO voltage bank 3
	VCCIO4	T3	PWR	+3.3V	IO voltage bank 4
	VCCIO4	L7	PWR	+3.3V	IO voltage bank 4
	VCCIO4	L10	PWR	+3.3V	IO voltage bank 4
	VCCIO4	T14	PWR	+3.3V	IO voltage bank 4
	GND	A1	PWR	GND	digital Gnd
	GND	A16	PWR	GND	digital Gnd
	GND	A5	PWR	GND	digital Gnd
	GND	A12	PWR	GND	digital Gnd
	GND	F6	PWR	GND	digital Gnd
	GND	F8	PWR	GND	digital Gnd
	GND	F9	PWR	GND	digital Gnd
	GND	F11	PWR	GND	digital Gnd
	GND	G7	PWR	GND	digital Gnd
	GND	G9	PWR	GND	digital Gnd
	GND	G11	PWR	GND	digital Gnd
	GND	H8	PWR	GND	digital Gnd
	GND	H10	PWR	GND	digital Gnd
	GND	J7	PWR	GND	digital Gnd
	GND	J9	PWR	GND	digital Gnd
	GND	K6	PWR	GND	digital Gnd
	GND	K8	PWR	GND	digital Gnd
	GND	K10	PWR	GND	digital Gnd
	GND	L6	PWR	GND	digital Gnd
	GND	L8	PWR	GND	digital Gnd
	GND	L9	PWR	GND	digital Gnd
	GND	L11	PWR	GND	digital Gnd
	GND	T1	PWR	GND	digital Gnd
	GND	T5	PWR	GND	digital Gnd
	GND	T12	PWR	GND	digital Gnd
	GND	T16	PWR	GND	digital Gnd

9. CPLD for external UARTs

A 2nd CPLD U2 is implemented to allow usage of the board without IP cores in the FPGA. This CPLD ispMACH4064 generates all signals for the external UART, audio channel and touch screen control. This CPLD is cheaper than the FPGA and needs no configuration after power up. Reprogramming can be done with JTAG booster or Lattice cables.

9.1. Usage

A9M9750 / 9360 8-bit data, 8-bit address interface. Control signals are EXT_CS0#, EXT_CS2#, EXT_CS3#, WAIT#, OE#, WE#, DMA0REQ and DMA0ACK, IRQ2 and RSTOUT#.

Generation UART signals UART_CS0..3#, UART_INT0..3, UART_IOR# and UART_IOW#.

Glue logic for emulation of I2S and L3 bus with SPIB and GPIO of the module using the signals L3MODE, SPIB_EN#, SPIB_CLK, AUD_L3_SDA, AUD_L3_SCL

Generation of 4.096MHz for AUD_CLK, 18.432MHz for UART_CLK and 3.6864MHz for IrDA_CLK

Touch. Needs control of PENIRQ# by the module.

9.2. Memory Map CPLD

see A9M9750DEV_1_logic_spec_V01.doc from spain.

9.3. Pinning CPLD

Pin	ispMACH4064 Pin Name	Type	Usage on developer board	comment
1	Gnd	PWR	Gnd	
2	TDI	prog	isp_TDI	Reprog. CPLD
3	A8	I	RSTOUT#	reset input
4	A9	O	WAIT#	external WAIT
5	A10	I	EXT_CS2#	ext chip sel
6	A11	I	EXT_CS3#	ext chip sel
7	Gnd	PWR	Gnd	
8	A12	I	EXT_CS0#	ext chip sel
9	A13	I	EXT_OE#	read signal
10	A14	I	WE#	write signal
11	A14	O	IRQ2	interrupt
12	I	input	nc	
13	+3.3V	PWR	+3.3V	
14	B15	O	**wire to AUD_WS**	**patch (_1)**
15	B14	I	nc	reserve
16	B13	I	nc	reserve
17	B12	I	nc	reserve
18	Gnd	PWR	Gnd	
19	B11	I	DMA0_ACK#	DMA
20	B10	O	DMA0_REQ	DMA
21	B9	O	SPIB_CLK	SPI B master
22	B8	O	SPIB_EN#	SPI B master

23	I	input	nc	
24	TCK	prog	isp_TCK	Reprog. CPLD
25	+3.3V	PWR	+3.3V	
26	Gnd	PWR	Gnd	
27	I	input	nc	
28	B7	I	A7	address bus
29	B6	I	A6	
30	B5	I	A5	
31	B4	I	A4	
32	Gnd	PWR	Gnd	
33	+3.3V	PWR	+3.3V	
34	B3	I	A3	
35	B2	I	A2	
36	B1	I	A1	
37	B0	I	A0	
38	CLK1/I	clk	36.864MHz	UART, IrDA clocks
39	CLK2/I	clk	11.2896MHz	Audio clock
40	+3.3V	PWR	+3.3V	
41	C0	O	UART_CLK	clk ext UARTs
42	C1	O	UART_IOR#	read ext UART
43	C2	O	UART_IOW#	write ext UART
44	C3	O	UART_RESET	RESET ext UART
45	+3.3V	PWR	+3.3V	
46	Gnd	PWR	Gnd	
47	C4	O	UART_CS0#	CS# ext UART chan 0
48	C5	O	UART_CS1#	CS# ext UART chan 1
49	C6	O	UART_CS2#	CS# ext UART chan 2
50	C7	O	UART_CS3#	CS# ext UART chan 3
51	Gnd	PWR	Gnd	
52	TMS	prog	isp_TMS	Reprog. CPLD
53	C8	I	UART_INT0	interrupt ext UARTch 0
54	C9	I	UART_INT1	interrupt ext UARTch 1
55	C10	I	UART_INT2	interrupt ext UARTch 2
56	C11	I	UART_INT3	interrupt ext UARTch 3
57	Gnd	PWR	Gnd	
58	C12	I/O	nc	reserve
59	C13	I/O	nc	reserve
60	C14	I/O	nc	reserve
61	C15	O	3.6864MHz	clk IrDA
62	I	input	nc	
63	+3.3V	PWR	+3.3V	
64	D15	O	AUD_CLK	to audio stage
65	D14	O	AUD_L3_SCL	L3 clock
66	D13	I/O	AUD_L3_SDA	L3 data
67	D12	I/O	nc	reserve
68	Gnd	PWR	Gnd	
69	D11	I/O	nc	reserve
70	D10	O	nc	reserve
71	D9	I	nc	reserve
72	D8	I	nc	reserve
73	I	input	nc	
74	TDO	prog	isp_TDO	Reprog. CPLD
75	+3.3V	PWR	+3.3V	
76	Gnd	PWR	Gnd	
77	I	input	nc	
78	D7	I/O	nc	reserve
79	D6	I/O	nc	reserve
80	D5	I/O	nc	reserve

81	D4	I/O	nc	reserve
82	Gnd	PWR	Gnd	
83	+3.3V	PWR	+3.3V	
84	D3	I/O	nc	reserve
85	D2	I/O	nc	reserve
86	D1	I	PENIRQ#	Touch control
87	D0/GOE1	I/O	nc	reserve
88	CLK3/I	clk	nc	
89	CLK0/I	clk	33.333MHz	PLD clock
90	+3.3V	PWR	+3.3V	
91	A0/GOE0	I/O	D0	Data Bus
92	A1	I/O	D1	
93	A2	I/O	D2	
94	A3	I/O	D3	
95	+3.3V	PWR	+3.3V	
96	Gnd	PWR	Gnd	
97	A4	I/O	D4	
98	A5	I/O	D5	
99	A6	I/O	D6	
100	A7	I/O	D7	

10. Mechanics

The size of the board is selected, to support also the extended version of the module, with its additional connectors X3 and X4.

- board size 205x145mm.
- PCB ML6, SMD on both sides.
- Standard Module fits on 2 connectors X1,X2 with 120 pins each. Pitch 0.8mm.
- Additional connectors X3,X4 for extended Module with 60 pins each. Pitch 0.8mm

10.1. Standard Module

The module size is defined to 60 x 44mm. Two holes, for M2 screws, catercornered, are provided to enable fixing of the module at the base board.

Two board to board connectors are used on the module. Depending on the counterpart at the base board, different distances between module and base board can be realized. The least possible distance is 5mm.

Therefore the height of the parts mounted at the bottom side of the module should not exceed 2.5mm. The height of the parts mounted at the top side should not exceed 4.1mm.

Board-to-Board Distance h	Module Connector X1, X2			
	No. of Pins	**Qty**	**Supplier**	**Order No.**
8 mm	120	2	AMP Berg	177983-5 61082-121000

Base Board Connector X1, X2		
No. Of Pins	**Supplier**	**Order No.**
120	AMP Berg	179031-5 61083-124000

10.2. Extended Module

For further modules it might be necessary to have some additional hardware placed on the module, which will need more signal lines connected between module and base board, than actual available. To meet these future requirements, an extended board is defined, which has two additional board to board connectors with 60 pins each.

The size of the extended module is defined to 92 x 44mm. Two holes, for M2 screws, catercornered, are provided to enable fixing of the module at the base board.

Board-to-Board Distance h	Module Connector X3, X4			
	No. of Pins	**Qty**	**Supplier**	**Order No.**
8 mm	60	2	AMP Berg	177983-2 61082-061009

Base Board Connector X3, X4		
No. Of Pins	**Supplier**	**Order No.**
60	AMP Berg	179031-2 61083-064009

11. Appendix A: Module Pinning

11.1. Module A9M9750

See “Pin_Description_A9M9750_X.pdf” or “*.doc”.

11.2. Module A9M9360

See “Pin_Description_A9M9360_X.pdf” or “*.doc”.

12. Appendix B: Board to Board Connectors

Grey areas are standard pin locations, equal on all modules.

I = Input, O = Output, AI = Analog Input, P = Power

Check **ARM9 Module Pinning Table.xls** to get the latest information about the pinning.

12.1. System Connector X1

Pin	Signal	Type	Signal Name	Description
X1-1	GND	P	GND	
X1-2	RSTIN#	I	RSTIN#	Reset button
X1-3	PWRGOOD	O	PWRGOOD	System reset
X1-4	RSTOUT#	O	RESET_DONE	High when boot program loaded
X1-5	TCK	I	TCK	JTAG
X1-6	TMS	I	TMS	JTAG
X1-7	TDI	I	TDI	JTAG
X1-8	TDO	O	TDO	JTAG
X1-9	TRST#	I	TRST#	JTAG
X1-10	Conf0	I	DEBUGEN#	Debug Enable
X1-11	Conf1	I	NAND_FWP#	WP internal Flash
X1-12	Conf2	I	OCD_EN#	Enable On Chip Debugging
X1-13	Conf3	I	HCONF3	high=PCI Mode, low=CardBus
X1-14	Conf4	I	GPIO38	Software Configuration
X1-15	Conf5	I	GPIO39	Software Configuration
X1-16	Conf6	I	GPIO40	Software Configuration
X1-17	Conf7	I	GPIO41	Software Configuration
X1-18	SPIA_DO or TxDA	O	SPIA_DO (GPIO8)	SPI_DO touch
X1-19	SPIA_DI or RxDA	I	SPIA_DI (GPIO9)	SPI_DI touch
X1-20	GPIO10	O	GPIO10	free
X1-21	IRQ2	I	IRQ2 (GPIO11)	IRQ from FPGA
X1-22		O	FPGA_CS0# (GPIO12)	CS# FPGA Configuration EEPROM via U41 analog switch
X1-23		I	GPIO13	connected with 0R to RTC_INT# on Module
X1-24	SPIB_DO or TXDB	O	SPIB_DO (GPIO0)	SPI_DO audio
X1-25	SPIB_DI or RXDB	I	SPIB_DI (GPIO1)	SPI_DI audio
X1-26		O	DMA1_ACK# (GPIO2)	free
X1-27	DMA0_REQ	I	DMA0_REQ (GPIO3)	DMA0 control from FPGA
X1-28		O	AUD_L3_MODE (GPIO4)	audio L3 port control
X1-29		O	DMA0_ACK# (GPIO5)	DMA0 control to FPGA
X1-30		I	SPIA_CLK (GPIO6)	audio control, SPI slave mode
X1-31		I	SPIA_CE# (GPIO7)	audio control, SPI slave mode
X1-32		I	WAIT#	external WAIT#
X1-33		O	A24	System Memory Address Bus, also GPIO68 at A9M9360 module
X1-34		O	A25	also GPIO69 at A9M9360 module
X1-35		O	A26	n.a. with A9M9360 module
X1-36		O	A27	n.a. with A9M9360 module
X1-37		I/O	LCD_D0 (GPIO24)	LCD/TFT-Interface
X1-38		I/O	LCD_D1 (GPIO25)	
X1-39	GND	P	GND	
X1-40		I/O	LCD_D2 (GPIO26)	

Pin	Signal	Type	Signal Name	Description
X1-41		I/O	LCD_D3 (GPIO27)	
X1-42		I/O	LCD_D4 (GPIO28)	
X1-43		I/O	LCD_D5 (GPIO29)	
X1-44		I/O	LCD_D6 (GPIO30)	
X1-45		I/O	LCD_D7 (GPIO31)	
X1-46		I/O	LCD_D8 (GPIO32)	
X1-47		I/O	LCD_D9 (GPIO33)	
X1-48		I/O	LCD_D10 (GPIO34)	
X1-49		I/O	LCD_D11 (GPIO35)	
X1-50		I/O	LCD_D12 (GPIO36)	
X1-51		I/O	LCD_D13 (GPIO37)	
X1-52		I/O	LCD_D14 (GPIO38)	
X1-53		I/O	LCD_D15 (GPIO39)	
X1-54		I/O	LCD_D16 (GPIO40)	
X1-55		I/O	LCD_D17 (GPIO41)	
X1-56		O	FPGA_DCLK or USB_EXTPHY_D+ (GPIO42)	CLK FPGA Conf. EEPROM via U41 analog switch or USB device external PHY control
X1-57		I	FPGA_DATA0 or USB_EXTPHY_D- (GPIO43)	DO FPGA Conf. EEPROM via U41 analog switch or USB device external PHY control
X1-58		O	FPGA_ASDO or USB_EXTPHY_OE# (GPIO44)	DI FPGA Conf. EEPROM U41 analog switch or USB device external PHY control
X1-59		I	GPIO45 or USB_PHY_RXD	Control Push Button 1 or USB device external PHY control
X1-60		I	GPIO46	Control Push Button 2
X1-61		O	GPIO47	Debug LED
X1-62		I/O	LCD_PWREN (GPIO18)	switch for backlight inverter
X1-63		I/O	LCD_AC_BDE (GPIO22)	
X1-64		I/O	LCD_FRAME (GPIO21)	via 22R series resistor
X1-65		I/O	LCD_HSYNC (GPIO19)	via 22R series resistor
X1-66		I/O	LCD_CLK (GPIO20)	via 22R series resistor
X1-67		I/O	LCD_LEND GPIO23)	
X1-68		O	A0	System Memory Address Bus
X1-69		O	A1	
X1-70		O	A2	
X1-71		O	A3	
X1-72		O	A4	
X1-73		O	A5	
X1-74		O	A6	
X1-75		O	A7	
X1-76		O	A8	
X1-77		O	A9	
X1-78		O	A10	
X1-79	GND	P	GND	
X1-80		O	A11	
X1-81		O	A12	
X1-82		O	A13	
X1-83		O	A14	
X1-84		O	A15	
X1-85		O	A16	
X1-86		O	A17	
X1-87		O	A18	

Pin	Signal	Type	Signal Name	Description
X1-88		O	A19	
X1-89		O	A20	
X1-90		O	A21	
X1-91		O	A22	also GPIO66 at A9M9360
X1-92		O	EXT_OE#	
X1-93		O	WE#	
X1-94		O	A23	also GPIO67 at A9M9360
X1-95		O	EXT_CS0#	Chip select from Module
X1-96		O	EXT_CS2#	Chip select from Module
X1-97		O	EXT_CS3#	Chip select from Module
X1-98			nc	
X1-99	PWREN	I	3.3V power sequencing input	not supported at A9M9750_0 Protos
X1-100	BATT_FLT#		nc	not supported with A9M9750 and A9M9360 modules
X1-101		I	USB_EXTPHY_SUSP (GPIO48)	USB device external PHY control
X1-102		I	USBH_OVERCURR (GPIO16)	(USB_OVERCURRENT)
X1-103		O	EXT_BE0#	Upper Byte/Lower Byte Enable
X1-104		O	EXT_BE1#	
X1-105		O	EXT_BE2#	
X1-106		O	EXT_BE3#	
X1-107	SS0#	O	SPIA_EN# (GPIO15)	SPI touch
X1-108	SPI_Master IN		nc	
X1-109	SPI_Master OUT		nc	
X1-110	SPICLK	O	SPIA_CLK (GPIO14)	SPI touch
X1-111	IICSCL	O	IICSCL	I2C, also GPIO70 or A26 at A9M9360
X1-112	IICSDA	I/O	IICSDA	I2C, also GPIO71 or A27 at A9M9360
X1-113	USB_Enum	I/O	USBh_ENUM (GPIO17)	USB host, switches pull-up to USBP- or USBN line
X1-114	USBP	I/O	USB_iINTPHY_P	USB data +
X1-115	USBN	I/O	USB_INTPHY_N	USB data -
X1-116	VRTC	P	VRTC	Power for RTC
X1-117	GND	P	GND	
X1-118	+3.3V	P	+3.3V	+3.3V for Peripherals
X1-119	VLIO	P	VLIO	Power from Li-Ion Battery for Core Voltage Connected to 3.3V normally
X1-120	+3.3V	P	+3.3V	+3.3V for Peripherals

12.2. System Connector X2

Pin	Signal	Type	Signal Name	Description
X2-1			PCI_INTA#, CINT or NC	PCI Bus / CardBus with A9M9750 Module, NC with A9M9360 Module
X2-2	GND	P	GND	
X2-3		I	PCI_INTC#, CSTSCHG or NC	
X2-4		I	PCI_INTB#, CCLKRUN or NC	
X2-5		O	PCI_RESET# or NC	
X2-6		I	PCI_INTD# or NC	
X2-7		O	PCI_GNT0# or NC	connected with 0R to PCI_GNT1#
X2-8		P	Gnd	
X2-9		O	PCI_GNT1#, CGNT or NC	
X2-10		O	PCI_CLK_OUT or NC	
X2-11		O	PCI_GNT2#, CVS2 or NC	
X2-12		I	PCI_CLK_IN or NC	
X2-13		O	PCI_GNT3# , CVS3 or NC	
X2-14		P	Gnd	
X2-15		I/O	PCI_AD30 or NC	
X2-16		I	PCI_REQ0# or NC	Connected with 0R to PCI_REQ1#
X2-17		I	PCI_REQ1#, CREQ or NC	
X2-18		I	PCI_REQ2#, CCD2 or NC	
X2-19		I	PCI_REQ3#, CCD3 or NC	
X2-20		I/O	PCI_AD31 or NC	
X2-21		I/O	PCI_AD28 or NC	
X2-22		I/O	PCI_AD29 or NC	
X2-23		I/O	PCI_AD26 or NC	
X2-24		I/O	PCI_AD27 or NC	
X2-25		I/O	PCI_AD24 or NC	
X2-26		I/O	PCI_AD25 or NC	
X2-27		I	PCI_IDSEL or NC	IDSEL from arbiter
X2-28		O	PCI_CBE3# or NC	
X2-29		I/O	PCI_AD22 or NC	
X2-30		I/O	PCI_AD23 or NC	
X2-31		I/O	PCI_AD20 or NC	
X2-32		I/O	PCI_AD21 or NC	
X2-33		I/O	PCI_AD18 or NC	
X2-34		I/O	PCI_AD19 or NC	
X2-35		I/O	PCI_AD16 or NC	
X2-36		I/O	PCI_AD17 or NC	
X2-37		I/O	PCI_FRAME# or NC	
X2-38		I/O	PCI_CBE2# or NC	
X2-39		I/O	PCI_TRDY# or NC	
X2-40	GND	P	GND	
X2-41		I/O	PCI_IRDY# or NC	
X2-42		I/O	PCI_STOP# or NC	
X2-43		I/O	PCI_PAR or NC	

Pin	Signal	Type	Signal Name	Description
X2-44		I/O	PCI_DEVSEL# or NC	
X2-45		I/O	PCI_AD15 or NC	
X2-46		I/O	PCI_PERR# or NC	
X2-47		I/O	PCI_AD13 or NC	
X2-48		I/O	PCI_SERR# or NC	
X2-49		I/O	PCI_AD11 or NC	
X2-50		I/O	PCI_CBE1# or NC	
X2-51		I/O	PCI_AD9 or NC	
X2-52		I/O	PCI_AD14 or NC	
X2-53		I/O	PCI_CBE0# or NC	
X2-54		I/O	PCI_AD12 or NC	
X2-55		I/O	PCI_AD6 or NC	
X2-56		I/O	PCI_AD10 or NC	
X2-57		I/O	PCI_AD4 or NC	
X2-58		I/O	PCI_AD8 or NC	
X2-59		I/O	PCI_AD2 or NC	
X2-60		I/O	PCI_AD7 or NC	
X2-61		I/O	PCI_AD5 or NC	
X2-62		I/O	PCI_AD3 or NC	
X2-63		I/O	PCI_AD1 or NC	
X2-64		I/O	PCI_AD0 or NC	
X2-65		I	LCD_CLKIN or NC	external LCD clk for A9M9750 module, NC for A9M9360 module
X2-66	TPIN0	I	ETH_TPIN0	Ethernet 0 Input-
X2-67	LEDLNK0	O	ETH_LEDLNK0	Ethernet 0 Link/Activity LED
X2-68	TPIP0	I	ETH_TPIP0	Ethernet 0 Input+
X2-69	LEDH0		ETH_LEDH0	Ethrnet 0 10/100Mbit LED
X2-70	TPON0	O	ETH_TPON0	Ethernet 0 Output-
X2-71	ESD0		ETH_ESD0	Fibre Sensor Detect
X2-72	TPOP0	O	ETH_TPOP0	Ethernet 0 Output+
X2-73	EREF0	P	nc	not used
X2-74			nc	
X2-75			nc	
X2-76			nc	
X2-77			nc	
X2-78			nc	
X2-79			nc	
X2-80	GND	P	GND	
X2-81		I/O	D0	Data Bus
X2-82		I/O	D1	
X2-83		I/O	D2	
X2-84		I/O	D3	
X2-85		I/O	D4	
X2-86		I/O	D5	
X2-87		I/O	D6	
X2-88		I/O	D7	
X2-89		I/O	D8	
X2-90		I/O	D9	
X2-91		I/O	D10	
X2-92		I/O	D11	
X2-93		I/O	D12	
X2-94		I/O	D13	

Pin	Signal	Type	Signal Name	Description
X2-95		I/O	D14	
X2-96		I/O	D15	
X2-97		I/O	D16	
X2-98		I/O	D17	
X2-99		I/O	D18	
X2-100		I/O	D19	
X2-101		I/O	D20	
X2-102		I/O	D21	
X2-103		I/O	D22	
X2-104		I/O	D23	
X2-105		I/O	D24	
X2-106		I/O	D25	
X2-107		I/O	D26	
X2-108		I/O	D27	
X2-109		I/O	D28	
X2-110		I/O	D29	
X2-111		I/O	D30	
X2-112		I/O	D31	
X2-113		O	nc (A28)	Reserved Address Lines
X2-114		O	nc (A29)	
X2-115		O	nc (A30)	
X2-116		O	nc (A31)	
X2-117	CANTXD/CANH	O	CANTX0	A9M9750 / A9M9360 no CAN support
X2-118	CANRXD/CANL	I	CANRX0	A9M9750 / A9M9360 no CAN support
X2-119	CLKOUT	O	BCLKOUT0	Buffered Clockout0
X2-120	GND	P	GND	

12.3. System Connector X3

Pin	Signal	Type	Signal Name	Description
X3-1	GND	P	GND	
X3-2				
X3-3				
X3-4				
X3-5				
X3-6				
X3-7				
X3-8				
X3-9				
X3-10				
X3-11				
X3-12				
X3-13				
X3-14				
X3-15				
X3-16				
X3-17				
X3-18				
X3-19				
X3-20				
X3-21				

Pin	Signal	Type	Signal Name	Description
X3-22				
X3-23				
X3-24				
X3-25				
X3-26				
X3-27				
X3-28				
X3-29				
X3-30				
X3-31	GND	P	GND	
X3-32				
X3-33				
X3-34				
X3-35				
X3-36				
X3-37				
X3-38				
X3-39				
X3-40				
X3-41				
X3-42				
X3-43				
X3-44				
X3-45				
X3-46				
X3-47				
X3-48				
X3-49				
X3-50				
X3-51				
X3-52				
X3-53				
X3-54				
X3-55				
X3-56				
X3-57				
X3-58				
X3-59	GND	P	GND	
X3-60				

12.4. System Connector X4

Pin	Signal	Type	Signal Name	Description
X4-1				
X4-2	GND	P	GND	
X4-3				
X4-4				
X4-5				
X4-6				
X4-7				
X4-8				

Pin	Signal	Type	Signal Name	Description
X4-9				
X4-10				
X4-11				
X4-12				
X4-13				
X4-14				
X4-15				
X4-16				
X4-17				
X4-18				
X4-19				
X4-20				
X4-21				
X4-22				
X4-23				
X4-24				
X4-25				
X4-26				
X4-27				
X4-28				
X4-29				
X4-30	GND	P	GND	
X4-31				
X4-32				
X4-33				
X4-34				
X4-35				
X4-36				
X4-37				
X4-38				
X4-39				
X4-40				
X4-41				
X4-42				
X4-43				
X4-44				
X4-45				
X4-46				
X4-47				
X4-48				
X4-49				
X4-50				
X4-51				
X4-52				
X4-53				
X4-54				
X4-55				
X4-56				
X4-57				
X4-58				
X4-59				

Pin	Signal	Type	Signal Name	Description
X4-60	GND	P	GND	

13. Appendix C: Expansion Connectors

13.1. Module Connector X1 versus X10/X11 Expansion Pin Rows

Pin	X10, Row A	X10, Row B	X11, Row C	X11, Row D
1	GND	RSTIN#	PWRGOOD	RSTOUT#
2	TCK	TMS	TDI	TDO
3	TRST#	DEBUGEN#	NAND_FWP#	OCD_EN#
4	PCI/CardBus Mode	CONF4	CONF5	CONF6
5	CONF7	SPIA_DO	SPIA_DI	GPIO10
6	IRQ2	nc (GPIO12)	GPIO13	SPIB_DO
7	SPIB_DI	DMA1_ACK#	DMA0_REQ	AUD_L3_MODE
8	DMA0_ACK#	SPIB_CLK	SPIB_CE#	WAIT#
9	A24	A25	A26	A27
10	LCD_D0	LCD_D1	GND	LCD_D2
11	LCD_D3	LCD_D4	LCD_D5	LCD_D6
12	LCD_D7	LCD_D8	LCD_D9	LCD_D10
13	LCD_D11	LCD_D12	LCD_D13	LCD_D14
14	LCD_D15	LCD_D16	LCD_D17	GPIO42 (CLK FPGA EEPROM)
15	GPIO43 (DI FPGA EEPROM)	GPIO44 (DO FPGA EEPROM)	GPIO45 (Button 1)	GPIO46 (Button2)
16	GPIO47 (DEBUG LED)	LCD_PWREN	LCD_AC_BDE	LCD_FRAME
17	LCD_HSYNC	LCD_CLK	LCD_LEND	A0
18	A1	A2	A3	A4
19	A5	A6	A7	A8
20	A9	A10	GND	A11
21	A12	A13	A14	A15
22	A16	A17	A18	A19
23	A20	A21	A22	EXT_OE#
24	WE#	A23	CS0#	CS2#
25	CS3#	nc	PWR_EN (**)	nc (BATT_FLT#)
26	GPIO48 (DMA1_REQ)	GPIO16 (USBH_OVC#)	EXT_BE0#	EXT_BE1#
27	EXT_BE2#	EXT_BE3#	SPIA_CE#	nc
28	nc	SPIA_CLK	IICSCL	IICSDA
29	GPIO17 (USBH_ENUM#)	USB_INTPHY_P via R95	USB_INTPHY_N via R96	VRTC
30	GND	GND	VLIO	VLIO
31	-	-	-	-
32	3.3V_IN (*)	3.3V_IN (*)	3.3V_IN (*)	3.3V_IN (*)

(*) 3.3V_IN is unswitched 3.3V, +3.3V is switched with PWREN high

(**) Power Sequencing Control from Module

13.2. Module Connector X2 versus X20/X21 Expansion Pin Rows

A9M9360 Module has no PCI/CardBus interface, all signals with the prefix PCI are NC

Pin	X20, Row A	X20, Row B	X21, Row C	X21, Row D
1	PCI_INTA#	GND	PCI_INTC#	PCI_INTB#
2	PCI_RESET#	PCI_INTD#	PCI_GNT0#	Gnd
3	PCI_GNT1#	PCI_CLK_OUT	PCI_GNT2#	PCI_CLK_EXP
4	PCI_GNT3#	Gnd	PCI_AD30	PCI_REQ0#
5	PCI_REQ1#	PCI_REQ2#	PCI_REQ3#	PCI_AD31
6	PCI_AD28	PCI_AD29	PCI_AD26	PCI_AD27
7	PCI_AD24	PCI_AD25	PCI_IDSEL	PCI_CBE3#
8	PCI_AD22	PCI_AD23	PCI_AD20	PCI_AD21
9	PCI_AD18	PCI_AD19	PCI_AD16	PCI_AD17
10	PCI_FRAME#	PCI_CBE2#	PCI_TRDY#	Gnd
11	PCI_IRDY#	PCI_STOP#	PCI_PAR	PCI_DEVSEL#
12	PCI_AD15	PCI_PERR#	PCI_AD13	PCI_SERR#
13	PCI_AD11	PCI_CBE1#	PCI_AD9	PCI_AD14
14	PCI_CBE0#	PCI_AD12	PCI_AD6	PCI_AD12
15	PCI_AD4	PCI_AD8	PCI_AD2	PCI_AD7
16	PCI_AD5	PCI_AD3	PCI_AD1	PCI_AD0
17	LCD_CLKIN (**)	ETH_TPIN0 via R97	LEDLNK0	ETH_TPIP0 via R98
18	ETH_LEDH0	ETH_TPON0 via R99	ETH_ESD0	ETH_TPOP0 via R100
19	nc	nc	nc	nc
20	nc	nc	nc	GND
21	D0	D1	D2	D3
22	D4	D5	D6	D7
23	D8	D9	D10	D11
24	D12	D13	D14	D15
25	D16	D17	D18	D19
26	D20	D21	D22	D23
27	D24	D25	D26	D27
28	D28	D29	D30	D31
29	nc	nc	nc	nc
30	nc	nc	BCLKOUT0	GND
31	VLIO	VRTC	GND	GND
32	+3.3V	+3.3V	RSTIN#	PWRGOOD

(**) NC with A9M9360 module

13.3. Module Connector X3 vs Expansion ConnectorsX30, X31

Pin	X30 Row A	X30, Row B	X31, Row C	X31, Row D
1	Gnd	X3_2	X3_3	X3_4
2	X3_5	X3_6	X3_7	X3_8
3	X3_9	X3_10	X3_11	X3_12
4	X3_13	X3_14	X3_15	X3_16
5	X3_17	X3_18	X3_19	X3_20
6	X3_21	X3_22	X3_23	X3_24
7	X3_25	X3_26	X3_27	X3_28
8	X3_29	X3_30	Gnd	X3_32
9	X3_33	X3_34	X3_35	X3_36
10	X3_37	X3_38	X3_39	X3_40
11	X3_41	X3_42	X3_43	X3_44
12	X3_45	X3_46	X3_47	X3_48
13	X3_49	X3_50	X3_51	X3_52
14	X3_53	X3_54	X3_55	X3_56
15	X3_57	X3_58	Gnd	X3_60
16	+3.3V	+3.3V	VLIO	VLIO
17				
18				
19				
20				

13.4. Module Connector X4 vs Expansion Connector X40, X41

Pin	X40 Row A	X40, Row B	X41, Row C	X41, Row D
1	X4_1	Gnd	X4_3	X4_4
2	X4_5	X4_6	X4_7	X4_8
3	X4_9	X4_10	X4_11	X4_12
4	X4_13	X4_14	X4_15	X4_16
5	X4_17	X4_18	X4_19	X4_20
6	X4_21	X4_22	X4_23	X4_24
7	X4_25	X4_26	X4_27	X4_28
8	X4_29	Gnd	X4_31	X4_32
9	X4_33	X4_34	X4_35	X4_36
10	X4_37	X4_38	X4_39	X4_40
11	X4_41	X4_42	X4_43	X4_44
12	X4_45	X4_46	X4_47	X4_48
13	X4_49	X4_50	X4_51	X4_52
14	X4_53	X4_54	X4_55	X4_56
15	X4_57	X4_58	X4_59	Gnd
16	+3.3V	+3.3V	VLIO	VLIO
17				
18				
19				
20				

14. Appendix D: Expansion Connectors X10/X11 and X20/X21 for A9M9750

A9M9750_1 has PWREN as additional signal. This pin is n.c. at A9M9750_0

14.1. Module Connector X1 versus X10/X11 Extension Pin Rows

Pin	X10, Row A	X10, Row B	X11, Row C	X11, Row D
1	Gnd	RSTIN#	PWRGOOD	RSTOUT#
2	TCK	TMS	TDI	TDO
3	TRST#	CONF0/ DEBUGEN#	CONF1/ FWP#	CONF2/ BNDSCN_EN#
4	CONF3/ CARDBUS#	CONF4/ GPIO38/GENID:28	CONF5/ GPIO39/GENID:29	CONF6/ GPIO40/GENID:30
5	CONF7/ GPIO41/GENID:31	TXDA	RXDA	RTSA#
6	CTSA#	GPIO12 (p)	GPIO13	TXDB
7	RXDB	RTSB#	CTSB#	DTRB#
8	DSRB#	RIB#	DCDB#	WAIT#
9	A24	A25	A26	A27
10	GPIO24 (p)	GPIO25	Gnd	GPIO26
11	GPIO27	GPIO28	GPIO29	GPIO30
12	GPIO31	GPIO32	GPIO33	GPIO34
13	GPIO35	GPIO36 (p)	GPIO37 (p)	GPIO38 (p)
14	GPIO39 (p)	GPIO40 (p)	GPIO41 (p)	GPIO42
15	GPIO43	GPIO44 (p)	GPIO45	GPIO46
16	GPIO47	GPIO18	GPIO22	GPIO21
17	GPIO19 (p)	GPIO20 (p)	GPIO23	A0
18	A1	A2	A3	A4
19	A5	A6	A7	A8
20	A9	A10	Gnd	A11
21	A12	A13	A14	A15
22	A16	A17	A18	A19
23	A20	A21	A22	EXT_OE#
24	WE#	A23	EXT_CS0#	EXT_CS2#
25	EXT_CS3#	X1, pin 98	PWREN (only A9M9750_1,2)	X1, pin 100 (BATT_FLT#)
26	GPIO48	GPIO16 (USBH_OVC#)	EXT_BE0#	EXT_BE1#
27	EXT_BE2#	EXT_BE3#	SS0#	SPIM_DI
28	SPIM_DO	SPIM_CLK	IIC_SCL	IIC_SDA
29	GPIO17 (USBH_ENUM#)	USB_INTPHY_P	USB_INTPHY_N	VRTC
30	Gnd	Gnd	VLIO	VLIO
31	-	-	-	-
32	+3.3V_IN	+3.3V_IN	+3.3V_IN	+3.3V_IN

14.2. Module Connector X2 versus X20/X21 Extension Pin Rows

Important: Check at A9M9750_0 Prototypes (364) when using PCI if PCI_CLKIN and PCI_GNT2# are patched on the module

Pin	X20, Row A	X20, Row B	X21, Row C	X21, Row D
1	PCI_INTA#	Gnd	PCI_INTC#	PCI_INTB#
2	PCI_RESET#	PCI_INTD#	PCI_GNT1#	Gnd
3	PCI_GNT1#	PCI_CLKOUT	PCI_GNT2# **may be PCI_CLKIN at A9M9750_0**	PCI_CLKIN **may be PCI_GNT2# at A9M9750_0**
4	PCI_GNT3#	Gnd	PCI_AD30	PCI_REQ1#
5	PCI_REQ1#	PCI_REQ2#	PCI_REQ3#	PCI_AD31
6	PCI_AD28	PCI_AD29	PCI_AD26	PCI_AD27
7	PCI_AD24	PCI_AD25	PCI_IDSEL	PCI_CBE3#
8	PCI_AD22	PCI_AD23	PCI_AD20	PCI_AD21
9	PCI_AD18	PCI_AD19	PCI_AD16	PCI_AD17
10	PCI_FRAME#	PCI_CBE2#	PCI_TRDY#	Gnd
11	PCI_IRDY#	PCI_STOP#	PCI_PAR	PCI_DEVSEL#
12	PCI_AD15	PCI_PERR#	PCI_AD13	PCI_SERR#
13	PCI_AD11	PCI_CBE1#	PCI_AD9	PCI_AD14
14	PCI_CBE0#	PCI_AD12	PCI_AD6	PCI_AD10
15	PCI_AD4	PCI_AD8	PCI_AD2	PCI_AD7
16	PCI_AD5	PCI_AD3	PCI_AD1	PCI_AD0
17	LCD_CLKIN	ETH_TPIN via R97	LEDLNK0	ETH_TPIP via R103
18	LEDH0	ETH_TPON via R98	ESD0	ETH_TPON via R104
19	X2 pin73 (EREF0)	X2 pin 74	X2 pin 75	X2 pin 76
20	X2 pin 77	X2 pin 78	X2 pin 79	Gnd
21	D0	D1	D2	D3
22	D4	D5	D6	D7
23	D8	D9	D10	D11
24	D12	D13	D14	D15
25	D16	D17	D18	D19
26	D20	D21	D22	D23
27	D24	D25	D26	D27
28	D28	D29	D30	D31
29	X2 pin 113 (A28)	X2 pin 114 (A29)	X2 pin 115 (A30)	X2 pin 116 (A31)
30	CANTX0	CANRX0	CLKOUT	Gnd
31	VLIO	VRTC	Gnd	Gnd
32	+3.3V	+3.3V	RSTIN#	PWRGOOD

15. Appendix E: Expansion Connectors X10/X11 and X20/X21 for A9M9360

15.1. Module Connector X1 versus X10/X11 Extension Pin Rows

Pin	X10, Row A	X10, Row B	X11, Row C	X11, Row D
1	Gnd	RSTIN#	PWRGOOD	RSTOUT#
2	TCK	TMS	TDI	TDO
3	TRST#	CONF0/ DEBUGEN#	CONF1/ FWP#	CONF2/ BNDSCN_EN#
4	CONF3/ n.c.	CONF4/ GPIO38/GENID:28	CONF5/ GPIO39/GENID:29	CONF6/ GPIO40/GENID:30
5	CONF7/ GPIO41/GENID:31	TXDA	RXDA	RTSA#
6	CTSA#	GPIO12 (p)	GPIO13	TXDB
7	RXDB	RTSB#	CTSB#	DTRB#
8	DSRB#	RIB#	DCDB#	WAIT#
9	A24	A25	n.c. (A26)	n.c. (A27)
10	GPIO24 (p)	GPIO25	Gnd	GPIO26
11	GPIO27	GPIO28	GPIO29	GPIO30
12	GPIO31	GPIO32	GPIO33	GPIO34
13	GPIO35	GPIO36 (p)	GPIO37 (p)	GPIO38 (p)
14	GPIO39 (p)	GPIO40 (p)	GPIO41 (p)	GPIO42
15	GPIO43	GPIO44 (p)	GPIO45	GPIO46
16	GPIO47	GPIO18	GPIO22	GPIO21
17	GPIO19 (p)	GPIO20 (p)	GPIO23	A0
18	A1	A2	A3	A4
19	A5	A6	A7	A8
20	A9	A10	Gnd	A11
21	A12	A13	A14	A15
22	A16	A17	A18	A19
23	A20	A21	A22	EXT_OE#
24	WE#	A23	EXT_CS0#	EXT_CS2#
25	EXT_CS3#	NC (CS3#)	PWREN	n.c. (BATT_FLT#)
26	GPIO48	GPIO16 (USBH_OVC#)	EXT_BE0#	EXT_BE1#
27	EXT_BE2#	EXT_BE3#	GPIO15 (SS0#)	n.c. (SPIA_MISO)
28	n.c. (SPIA_MOSI)	GPIO14 (SPIA_CLK)	IIC_SCL (GPIO70)	IIC_SDA (GPIO71)
29	GPIO17 (p) (USBH_ENUM#)	USB_INTPHY_P via R95	USB_INTPHY_N via R96	VRTC
30	Gnd	Gnd	VLIO	VLIO
31	-	-	-	-
32	+3.3V_IN	+3.3V_IN	+3.3V_IN	+3.3V_IN

15.2. Module Connector X2 versus 20/X21 Extension Pin Rows

Pin	X20, Row A	X20, Row B	X21, Row C	X21, Row D
1		Gnd		
2				
3				
4				
5				
6				
7				
8				
9				
10				Gnd
11				
12				
13				
14				
15				
16				
17		ETH_TPIN via R97	LEDLNK0	ETH_TPIP via R103
18	LEDH0	ETH_TPON via R98	ESD0	ETH_TPOP via R104
19	X2 pin73 (EREF0)	X2 pin 74	X2 pin 75	X2 pin 76
20	X2 pin 77	X2 pin 78	X2 pin 79	Gnd
21	D0	D1	D2	D3
22	D4	D5	D6	D7
23	D8	D9	D10	D11
24	D12	D13	D14	D15
25	D16	D17	D18	D19
26	D20	D21	D22	D23
27	D24	D25	D26	D27
28	D28	D29	D30	D31
29	X2 pin 113 (A28)	X2 pin 114 (A29)	X2 pin 115 (A30)	X2 pin 116 (A31)
30	CANTX0	CANRX0	CLKOUT	Gnd
31	VLIO	VRTC	Gnd	Gnd
32	+3.3V	+3.3V	RSTIN#	PWRGOOD

16. Appendix F: General Connectors

16.1. X5: CAN Connector Channel 0

Header 2X5 pin male, RM2.54, signals have 5V levels. Depending on board population either differential signals CANL0/CANH0 or the signals CANTX0/CANRX0 are provided.

Pin	Function	Comment
1		
2	CANL0/CANRX0	
3	Gnd	
4		
5		
6	Gnd	
7	CANH0/CANTX0	
8		
9		
10		

16.2. X6: CAN Connector Channel 1

Header 2X5 pin male, RM2.54, signals have 5V levels. Depending on board population either differential signals CANL1/CANH1 or the signals CANTX1/CANRX1 are provided.

Pin	Function	Comment
1		
2	CANL1/CANRX1	
3	Gnd	
4		
5		
6	Gnd	
7	CANH1/CANTX1	
8		
9		
10		

16.3. X7: External 5V Power

4pin

Pin	Function	Comment
1	+5V	
2	GND	
3	GND	
4	+12V	not used on developers board

16.4. X8: Header COM1

Header 2X5 pin male, RM2.54, signals have 3.3V levels

Pin	Function	Comment
1	EDCD1#	
2	ERXD1	
3	ETXD1	
4	EDTR1#	
5	GND	
6	EDSR1#	
7	ERTS1#	
8	ECTS1#	
9	ERI1#	
10	+3.3V	

16.5. X9: ByteBlaster Connector Configuration EEPROM FPGA

Header 2X5 pin female, RM2.54, signals have 3.3V levels, allows usage of ALTERA ByteBlaster II cable

Pin	Function	Comment
1	DCLK	serial clock from FPGA to EEPROM
2	Gnd	Power
3	FPGA_CONF_DONE	high means Configuration successful
4	+3.3V	Power to cable
5	FPGA_CONFIG#	Start Configuration with rising edge
6	FPGA_CE#	Disable FPGA by pulling high
7	FPGA_DATAO	Data out from EEPROM
8	FPGA_CS0#	Chip select to EEPROM
9	FPGA_ASDO	Data in to ASDI EEPROM
10	Gnd	Gnd

16.6. X12: JTAG Booster Connector

8pin, 2.54mm, single row, Signals have 3.3V TTL levels

Pin	Function	Comment
1	TCK	
2	GND	
3	TMS	
4	TRST#	
5	NC	
6	TDI	
7	TDO	
8	+3.3V	

16.7. X13: Connector JTAG Multi-ICE

20pin, 2.54mm, dual row, signals have 3.3V TTL levels

Pin	Function	Comment	Pin	Function	Comment
1	NC		2	+3.3V	
3	TRST#		4	GND	
5	TDI		6	GND	
7	TMS		8	GND	
9	TCK		10	GND	
11	RTCK	via 0R to TCK	12	GND	
13	TDO		14	GND	
15	SRST#		16	GND	
17	NC		18	GND	
19	NC		20	GND	

16.8. X14: Connector USB Host

4pin Type A

Pin	Function	Comment
1	+5V	
2	USBH_N	
3	USBH_P	
4	GND	

16.9. X15: Connector USB Device

4pin Type B

Pin	Function	Comment
1	NC	
2	USBD_N	
3	USBD_P	
4	GND	

16.10. X16: Connector COMB

D-SUB 9 pin male, signals have RS232 levels, connected to external UART channel 1

Pin	Function	Comment
1	EDCDB#	
2	ERXDB	
3	ETXDB	
4	EDTRB#	
5	GND	
6	EDSRB#	
7	ERTSB#	
8	ECTSB#	
9	ERI1B#	

16.11. X17: Ethernet Connector 10/100Mb

RJ45 8 pin

Pin	Function	Comment
1	TX+	
2	TX-	
3	RX+	
4	VGND1	
5	VGND1	
6	RX-	
7	VGND2	
8	VGND2	

16.12. X18: Connector COMA

D-SUB 9 pin male, signals have RS232 levels, connected to external UART channel 0

Pin	Function	Comment
1	EDCDA#	
2	ERXDA	
3	ETXDA	
4	EDTRA#	
5	GND	
6	EDSRA#	
7	ERTSA#	
8	ECTSA#	
9	ERIA#	

16.13. X19: Header COM0

Header 2X5 pin male, RM2.54, signals have 3.3V levels

Pin	Function	Comment
1	EDCD0#	
2	ERXD0	
3	ETXD0	
4	EDTR0#	
5	GND	
6	EDSR0#	
7	ERTS0#	
8	ECTS0#	
9	ERI0#	
10	+3.3V	

16.14. X22: Connector Audio Line Out / Headphones

3.5mm audio jack 5 position stereo

Pin	Function	Comment
1	Gnd	
2	I2SOUTR	Out right
3	nc	switch right
4	nc	switch left
5	I2SOUTL	Out left

16.15. X23: Connector Audio Microphone

3.5mm audio jack 5 position stereo

Pin	Function	Comment
1	Gnd	
2	nc (I2SMIC)	In right, connected with optional 0R to IS2MIC
3	nc (SWR)	switch right, nc
4	SWL	switch left, connected with 0R to Gnd
5	I2SMIC	In left, connected to I2SMIC

16.16. X24: Connector Audio Line In

3.5mm audio jack 5 position stereo

Pin	Function	Comment
1	Gnd	
2	I2SLINER	In right
3	SWR	switch right, connected with 0R to Gnd
4	SWL	switch left, connected with 0R to Gnd
5	I2SLINEL	In left

16.17. X25: Connector LCD

40pin dual row connector, RM2.54

Pin	Function	Comment	Pin	Function	Comment
1	GND		2	LCD_HCLK	
3	HSYNC		4	VSYNC	
5	GND		6	LCD_D0	
7	LCD_D1		8	LCD_D2	
9	LCD_D3		10	LCD_D4	
11	LCD_D5		12	GND	
13	LCD_D6		14	LCD_D7	
15	LCD_D8		16	LCD_D9	
17	LCD_D10		18	LCD_D11	
19	GND		20	LCD_D12	
21	LCD_D13		22	LCD_D14	
23	LCD_D15		24	LCD_D16	
25	LCD_D17		26	GND	
27	LCD_AC_DBE		28	+3.3V	
29	+3.3V		30	LCDVF0	
31	LCDVF1		32	LCDVF2	
33	GND		34	nc	
35	nc		36	nc	
37	nc		38	nc	
39	LCD_PWREN		40	GND	

16.18. X26: Header COM3

Header 2X5 pin male, RM2.54, signals have 3.3V levels

Pin	Function	Comment
1	EDCD3#	
2	ERXD3	
3	ETXD3	
4	EDTR3#	
5	GND	
6	EDS3#	
7	ERTS3#	
8	ECTS3#	
9	ERI3#	
10	+3.3V	

16.19. X27: Connector SPI Channel A (Touch)

Header 2X5 pin male, RM2.54, signals have 3.3V levels, connected to internal SPI channel A

Pin	Function	Comment
1	nc	
2	SPIA_EN#	
3	nc	
4	SPIA_CLK	
5	nc	
6	SPIA_DO	
7	nc	
8	SPIA_DI	
9	nc	
10	PENIRQ#	

16.20. X28: Mini PCI Socket

Mini-PCI, Typ3 Conn., 124pin, 90°

All signals with prefix PCI_ are NC with A9M9360 Module

Pin	Function	Pin	Function
1	nc (TIP)	2	nc (RING)
	KEY		KEY
3	nc (RJ45-3)	4	nc (RJ45-1)
5	nc (RJ45-6)	6	nc (RJ45-2)
7	nc (RJ45-7)	8	nc (RJ45-4)
9	nc (RJ45-8)	10	nc (RJ45-5)
11	LED1_GRNP	12	LED2_YELP
13	LED1_GRNN	14	LED2_YELN
15	CHSGND (connected with 0R to Gnd)	16	nc (RESERVED1)
17	nc (PCI_INTB#)	18	nc (+5V/100mA)
19	+3.3V_PCI	20	PCI_INTA#
21	nc (RESERVED2)	22	nc (RESERVED3)
23	Gnd	24	+3.3V_PCI (3.3VAUX)
25	PCI_CLKOUT0	26	PCI_RESET#
27	Gnd	28	+3.3V_PCI
29	MPCI_REQ1#	30	PCI_GNT1#
31	+3.3V_PCI	32	Gnd
33	PCI_AD31	34	nc (PME#)
35	PCI_AD29	36	nc (RESERVED4)
37	Gnd	38	PCI_AD30
39	PCI_AD27	40	+3.3V_PCI
41	PCI_AD25	42	PCI_AD28
43	nc (RESERVED5)	44	PCI_AD26
45	PCI_CBE3#	46	PCI_AD24
47	PCI_AD23	48	IDSEL slot, connected to PCI_AD16
49	Gnd	50	Gnd
51	PCI_AD21	52	PCI_AD22
53	PCI_AD19	54	PCI_AD20
55	Gnd	56	PCI_PAR
57	PCI_AD17	58	PCI_AD18
59	PCI_CBE2#	60	PCI_AD16
61	PCI_IRDY#	62	Gnd
63	+3.3V_PCI	64	PCI_FRAME#
65	PCI_CLKRUN#	66	PCI_TRDY#
67	PCI_SERR#	68	PCI_STOP#
69	Gnd	70	+3.3V_PCI
71	PCI_PERR#	72	PCI_DEVSEL#
73	PCI_CBE1#	74	Gnd
75	PCI_AD14	76	PCI_AD15
77	Gnd	78	PCI_AD13
79	PCI_AD12	80	PCI_AD11
81	PCI_AD10	82	Gnd
83	Gnd	84	PCI_AD9
85	PCI_AD8	86	PCI_CBE0#
87	PCI_AD7	88	+3.3V_PCI
89	+3.3V_PCI	90	PCI_AD6
91	PCI_AD5	92	PCI_AD4
93	nc (RESERVED6)	94	PCI_AD2
95	PCI_AD3	96	PCI_AD0
97	nc (+5V/100mA)	98	nc (RESERVED_WIP1)

99	PCI_AD1	100	nc (RESERVED_WIP2)
101	Gnd	102	Gnd
103	nc (AC_SYNC)	104	PCI_M66EN
105	nc (AC_SDATA_IN)	106	nc (AC_SDATA_OUT)
107	nc (AC_BIT_CLK)	108	nc (AC_CODEC_ID0#)
109	nc (AC_CODEC_ID1#)	110	nc (AC_RESET#)
111	nc (MOD_AUDIO_MON)	112	nc (RESERVED7)
113	nc (AUDIO_GND)	114	Gnd
115	nc (SYS_AUDIO_GND)	116	nc (SYS_AUDIO_IN)
117	nc (SYS_AUDIO_OUT_GND)	118	nc (SYS_AUDIO_IN_GND)
119	nc (AUDIO_GND)	120	nc (AUDIO_GND)
121	nc (RESERVED8)	122	PCI_MPCIACT#
123	nc (VCC5VA)	124	+3.3V_PCI (3.3VAUX)

16.21. X29: Compact Flash Socket

Compact Flash Connector Type II, 50 pole

Pin	Function	Pin	Function
1	Gnd	26	CF_CD1#
2	CF_D3	27	CF_D11
3	CF_D4	28	CF_D12
4	CF_D5	29	CF_D13
5	CF_D6	30	CF_D14
6	CF_D7	31	CF_D15
7	CF_CE1#	32	CF_CE2#
8	CF_A10	33	nc (VS1)
9	CF_OE#	34	CF_IORD#
10	CF_A9	35	CF_IOWR#
11	CF_A8	36	CF_WE#
12	CF_A7	37	CF_RDY/IRQ#
13	+3.3V_PCI	38	+3.3V_PCI
14	CF_A6	39	Gnd (MSTR#/SLAVE)
15	CF_A5	40	nc (VS2)
16	CF_A4	41	CF_RESET
17	CF_A3	42	CF_WAIT#
18	CF_A2	43	nc (INPACK#)
19	CF_A1	44	CF_REG#
20	CF_A0	45	nc (BVD2)
21	CF_D0	46	nc (BVD1)
22	CF_D1	47	CF_D8
23	CF_D2	48	CF_D9
24	CF_WP/IOCS16#	49	CF_D10
25	nc (CF_CD2#)	50	Gnd

16.22. X32: Header COM2

Header 2X5 pin male, RM2.54, signals have 3.3V levels

Pin	Function	Comment
1	EDCD2#	
2	ERXD2	
3	ETXD2	
4	EDTR2#	
5	GND	
6	EDSR2#	
7	ERTS2#	
8	ECTS2#	
9	ERI2#	
10	+3.3V	

16.23. X33: ispMACH Connector

8pin, 2.54mm, single row, Signals have 3.3V TTL levels

Pin	Function	Comment
1	TCK	
2	GND	
3	TMS	
4	nc	
5	nc	
6	TDI	
7	TDO	
8	+3.3V	

17. Appendix G: Jumper Functions

Number	Function	Comments
J1	Open: V_{RTC} not buffered Closed: V_{RTC} battery buffered with G1	battery buffering RTC
J2	Open: Receiver channels U4 MAX3241 disabled or MAX3243 enabled Closed: Receiver channels U4 MAX3241 enabled or MAX3243 disabled	RS232 driver control channel A
J3	Open: Receiver channels U5 MAX3241 disabled or MAX3243 enabled Closed: Receiver channels U5 MAX3241 enabled or MAX3243 disabled	RS232 driver control channel B
J4_1	1-2: closed 3-4: open 5-6: closed 7-8: open J16 closed, J17 open	USB selection INTPHY host EXTPHY not used
J4_2	1-2: open 2-3: closed 5-6: open 6-7: closed J16 closed, J17 open	USB selection INTPHY device EXTPHY not used
J4_3	1-2: closed 3-4: closed 5-6: closed 7-8: closed J16 closed, J17 closed	USB selection INTPHY host EXTPHY selection device
J4_4	1-2: X 3-4: X 5-6: X 7-8: X J16 open, J17 closed	FPGA remote reprogramming, USB selection INTPHY host or device EXTPHY not used
J5	open: RXD3 connected to RS232 header	RS232/IrDA selection RXD3

Number	Function	Comments
	closed: RXD3 connected to IrDA converter	
J8	Selection LCD display modes R/L (not fitted on variant 0376)	horizontal LCD display 0 normal 1 left/right reversed
J9	Selection LCD display modes U/D (not fitted on variant 0376)	vertical LCD display 0 up/down reversed 1 normal
J10	Selection LCD display modes V/Q (not fitted on variant 0376)	LCD data handling 0 QVGA data used 1 VGA data used
J11	Closed: CAN Termination channel 0 active	close only if CAN driver U13 populated
J12	Closed: CAN Termination channel 1 active	close only if CAN driver U14 populated
J13	Open: LED LE4 open for free usage Closed: LED LE4 connected to GPIO47	Debug LED control
J16,17	0= closed, 1= open, X= both possible J17=0, J16=0: Connect GPIO12, 42..48 to USB_PHY J17=0, J16=1: Connect remote interface GPIO12, 42..44 for FPGA Configuration EEPROM programming J17=1, J16=X: GPIO12, 42..48 disconnected	Selection USB_EXTPHY (only A9M9360) and FPGA Configuration EEPROM remote programming

18. Appendix J: Software Hints

WinCE and Linux is supported for the A9M9750 / A9M9360 modules. The dev kit with module, development board and software has to support several interfaces. The software drivers will have to be adapted, partly new written.

18.1. LCD

Same LCD as for A9M2410 development board.

18.2. Touch

Touch controller of LCD board is connected to SPI controller channel A of the NS9750 or NS9360 CPU.

18.3. RS232, IrDA

Usage of external UARTs on development board; channel 3 can be set with jumpers to IrDA mode.

18.4. USB with internal PHY

Either host or device mode possible(A9M9750, A9M9360). When using with 2nd channel (only A9M9360), set to host mode.

18.5. USB with external PHY (only A9M9360)

Set to device mode.

18.6. CAN

CAN controller in FPGA is different from 82C900.

18.7. Ethernet

10/100Mb interface on board.

18.8. Compact Flash

Same logic as for A9M2410.

18.9. Mini PCI

PCI arbiter in NS9750 CPU. Set to host mode. PCI patch may be supported in FPGA.

18.10. Audio Codec

Hardware similar to A9M2410DEV board. L3 bus clk and data from FPGA or CPLD with additional GPIO port L3MODE, SPI channel B is used for I2S emulation.

19. Verification

19.1. Not Tested Functions

19.1.1. IrDA

19.1.2. USB Host (A9M9750)

19.1.3. USB Host (A9M9360)

19.1.4. USB Device with internal PHY (A9M9750)

19.1.5. USB Device with internal PHY (A9M9360)

19.1.6. USB Device with external PHY (A9M9360)

19.1.7. Audio (FPGA)

19.1.8. CF Slot (A9M9750)

19.1.9. CF Slot (A9M9360)

19.1.10. MiniPCI Slot (A9M9750)

19.1.11. FPGA PCI Patch (FPGA, A9M9750)

19.1.12. External UARTs (FPGA)

19.2. Status Tested Functions

19.2.1. Internal UARTs

19.2.2. External UARTs (ST16C754)

19.2.3. SPI

19.2.4. CAN (FPGA)

19.2.5. Ethernet (A9M9750)

19.2.6. Ethernet (A9M9360)

19.2.7. LCD

19.2.8. Touch

19.2.9. External Interrupts (FPGA)

19.3. Known Bugs

See review_A9M9750DEV_2.txt in CAD\A9M9750DEV_2.