ConnectCore 9C/Wi-9C
Parallel Peripheral Port Application Note

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Change History

Revision	Date	Summary
01	8 JUN 07	DRAFT Copy for Internal Review
02	9 JUN 07	Added CS0 Base and mask settings
03	3 JUL 07	Made corrections to Signal Descriptions
04	3 JUL 07	Corrected spelling - "These" under Address_[7:0]

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1. Scope

The purpose of this document is to describe how to connect a peripheral to the CCX9C NS9360 module's CS0 parallel data port, and how to program Chip Select 0.

2. Overview

This 8-bit memory mapped interface is similar to the interface to a flash chip, where the NS9360 is the master. The interface was designed as a moderate to low speed parallel/SRAM style data bus. To access the External Memory Bus you will be using Chip Select 0 (CS0) on the NS9360.

3. Signal Description

This section briefly describes the signals that connect the two systems.

DATA_[7:0]
NS9360, buffered, bi-directional data bus. The 74LVCHR16245 buffer is enabled when CS0# is active low. Driven during write cycles at LVTTL voltage levels with +/-12ma drive. Drivers have 26 ohm, built-in series resistors. During read cycles the buffer inputs provide bus-hold. Inputs can be driven from either 3.3-V or 5-V devices.

ADDRESS_[7:0]
NS9360 buffered address lines. Output only. The 74LVCHR16245 buffer is enabled when CS0# is active low. These drivers have LVTTL voltage levels with +/-12ma drive, and have 26 ohm, built-in series resistors.
The connecting device should provide 10K pull-up resistors to prevent address line float during CS0# inactive times.

CS# /CS0#
NS9360 buffered Chip Select 0. Output, active low for both Read and Write cycles.
Driver is a NC7SZ32. LVTTL voltage levels with +/-24ma drive.

OE#
NS9360 buffered Output Enable. Output, active low for Read cycles only.
Driver is a NC7SZ32. LVTTL voltage levels with +/-24ma drive.

WE#
NS9360 buffered Write Enable. Output, active low for Write cycles only.
Driver is a NC7SZ32. LVTTL voltage levels with +/-24ma drive.

NOTE: Series resistors are recommended on the control lines to reduce EMI Transmissions.

4. Connection Example

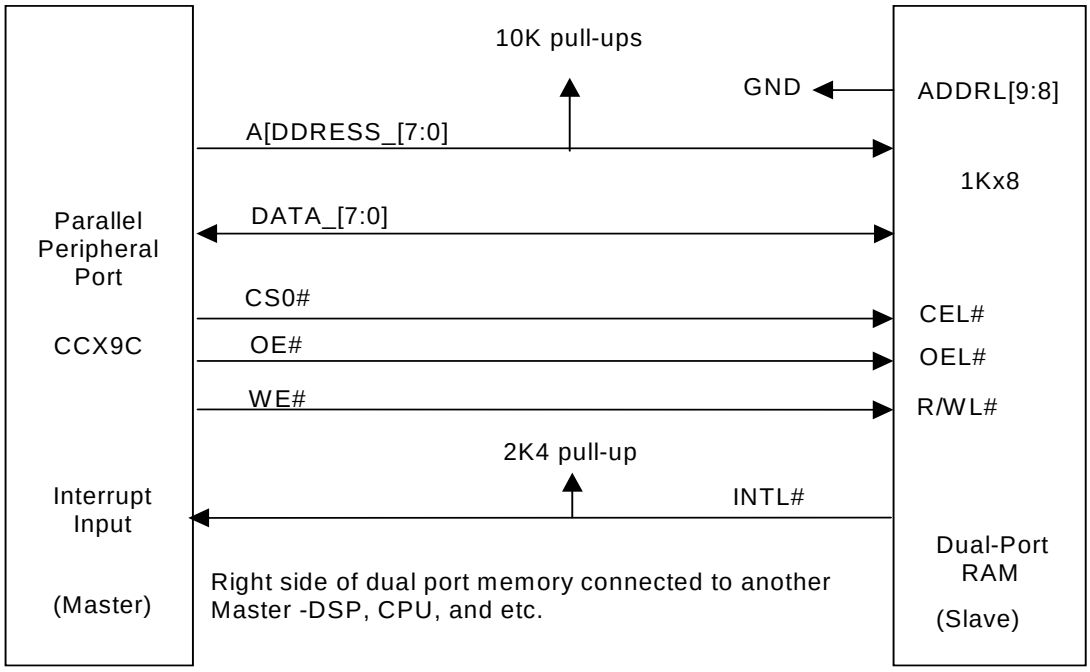


Figure 1 - Dual Port Memory Example

5. Read (Inbound) Wait States and OE# Delay

The WOEN and WTRD fields work together to determine how the CS# and OE# signals will behave during a static read cycle.

A070 0208 = WOEN
A070 020C = WTRD

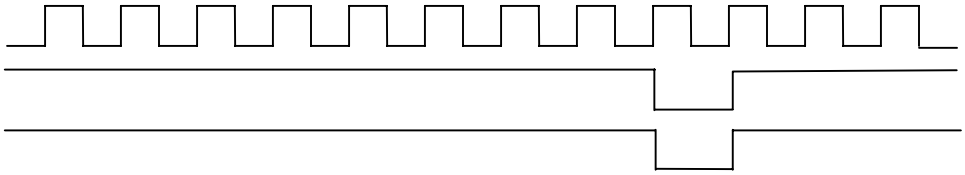
In all cases the CS0# signal will go high on the same clock edge as the OE# signal goes high. There is no setting of WOEN or WTRD that will affect this.

The CS0# and OE# signals will always be low for at least 1 clock cycle. The WTRD can be set to allow up to 32 clock cycles to be added to both the CS0# and OE# signals.

The WOEN field can be configured to force the OE# signal to go low after the after the CS# signal goes low.

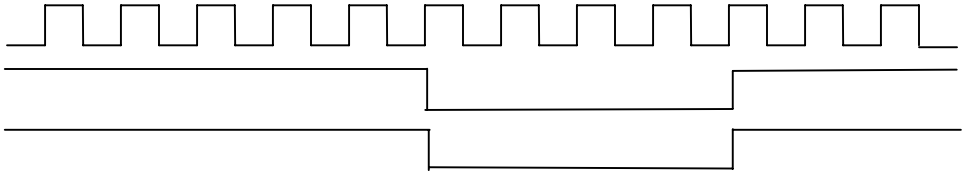
This is how the CS0# and OE# will behave if both fields are set to 0. The CS0# signal is low for 1 clock and the WE# signal is low for 1.

WTRD = 0
WOEN = 0



The WTRD field adds to the length of both signals. If the WTRD field were set to ‘3’ and the WOEN field were set to ‘0’, both the CS0# and OE# signals would increase by 3 clock cycles.

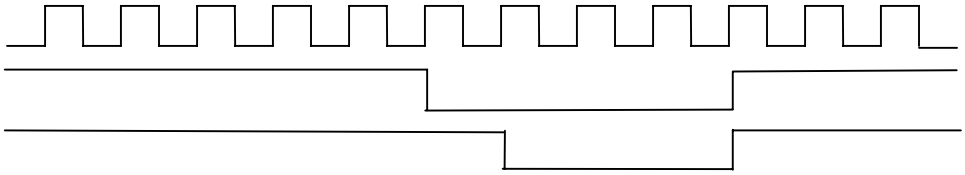
WTRD = 3
WOEN = 0



The WOEN field only affects the length of the OE# signal. It has no effect on the length of the CS0# signal. The WOEN field subtracts from the length of the OE# signal that was set with the WTRD field.

If the WTRD field remains at ‘3’ and the WOEN field were set to ‘1’, then 1 clock cycle would be subtracted from the leading edge of the OE# signal.

WTRD = 3
WOEN = 1



5.1 Read cycles from 8 Bit peripherals

The data width of each external memory bank must be configured by programming the appropriate bank configuration register (Static Memory Configuration 0–3). When the external memory bus is narrower that the transfer initiated from the current main bus master, the internal bus transfer takes several external bus transfers to complete.
For example, CS0 is configured as 8-bit wide memory and a 32-bit read is initiated, the AHB bus stalls while the memory controller reads four consecutive bytes from the memory. During these accesses, the static memory controller block demultiplexes the four bytes into one 32-bit word on the AHB bus.
Therefore:
A ***byte read*** will produce 1 memory cycle. Works for all.

A ***word read*** will produce 4 memory cycles with CS0# and OE# remaining solid low throughout all four read accesses. Address_[1:0] change for each access.

WARNING! Word and half word reads present a problem to peripherals which require CS0# and/or OE# to toggle on each byte. Dual port memory will track Address_[1:0] and should be O.K.

6. Write (Outbound) Wait States and WE# Delay

The WWEN and WTWR fields work together to determine how the CS# and WE# signals will behave during a static write cycle.

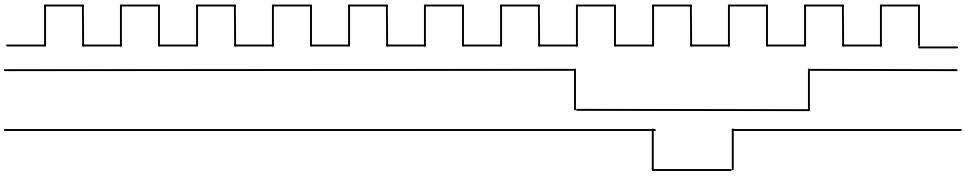
A070 0204 = WWEN
A070 0214 = WTWR
In all cases the CS0# signal will go high one clock cycle after the WE# signal goes high. There is no setting of WWEN or WTWR that will affect this.

The CS0# signal will always be low for at least 3 clock cycles. The WE# signal will be low for at least 1 clock cycle. The WTWR can be set to allow up to 32 clock cycles to be added to both the CS0# and WE# signals.

In all cases the WE# signal will go low at least one clock cycle after the CS# signal goes low. The WWEN field can be configured to force the WE# signal to go low more than one clock cycle after the after the CS# signal goes low.

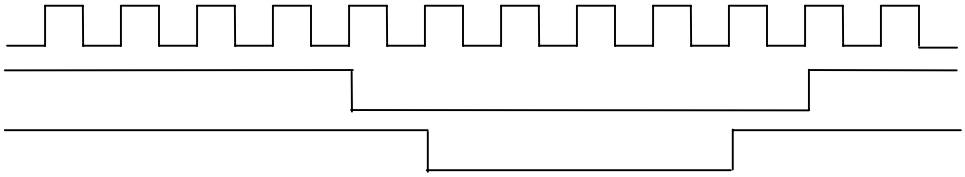
This is how the CS0# and WE# will behave if both fields are set to 0. The CS0# signal is low for 3 clocks and the WE# signal is low for 1.

WTWR = 0
WWEN = 0



The WTWR field adds to the length of both signals. If the WTWR field were set to ‘3’ and the WWEN field were set to ‘0’, both the CS0# and WE# signals would increase by 3 clock cycles.

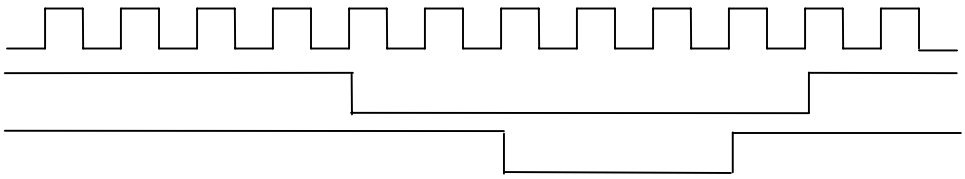
WTWR = 3
WWEN = 0



The WWEN field only affects the length of the WE# signal. It has no effect on the length of the CS0# signal. The WWEN field subtracts from the length of the WE# signal that was set with the WTWR field.

If the WTWR field remains at ‘3’ and the WWEN field were set to ‘1’, then 1 clock cycle would be subtracted from the leading edge of the WE# signal.

WTWR = 3
WWEN = 1



7. Static Memory Chip Select 0 Sample Configuration

This "example" inserts 3 wait states for both the reads and writes.
OE# is delayed 1 clock from the falling edge of CS0#; WE# is delayed 2 clocks

A070 0200
Static Memory configuration resister = 0x0000 0080
PB is a 1 to select WE# instead of byte_lane[0]# for writes.

A070 0204
WWEN Wait write enable (WAITWEN) = 1

A070 0208
WOEN Wait output enable (WAITOEN) = 1

A070 020C
WTRD Non-page mode read wait states or asynchronous page
mode read first access wait state (WAITRD) = 3

A070 0210
WTPG Asynchronous page mode read after the first wait state(WAITPAGE) = 2
Most peripherals do not support this mode.

A070 0214
WTWR Write wait states (WAITWR) = 3

A070 0218
WTTN Bus turnaround cycles (WAITTURN) = 1

A090 01F0 / 01F4
System Memory Chip Select 0 Static Memory Base and Mask registers
4K is the minimum address range

Base defaults to 0x40000 000
Note: Bits 11:0 are reserved.

MASK defaults to 0xF0000 000 for 256M with Chip Select disabled.
Change to 0xFFFFF 001 for 4K with Chip Select enabled
Note: Bits 11:1 are reserved; Bit 0 is the chip select enable

Or make this change to the BSP address table for CS0
mc 0x40000000:P 0x40000FFF:P, JAM, PWE, // CS0: 4K
Parallel Peripheral Port

8. SRAM timing parameters

M15-24, M27-28 are (+/- 2 ns) from the rising clock edge.

M25 data input setup time to rising clk = 10 ns Min.
Add to this number the delay time of the 74LVC16245 data buffer (Typical 5 ns)

M26 data input hold time to rising clk = 0 ns Min.

Note: CPU clock/2 = 77.5Mhz. It is not available on the Module's edge connector.

9. Read Timing

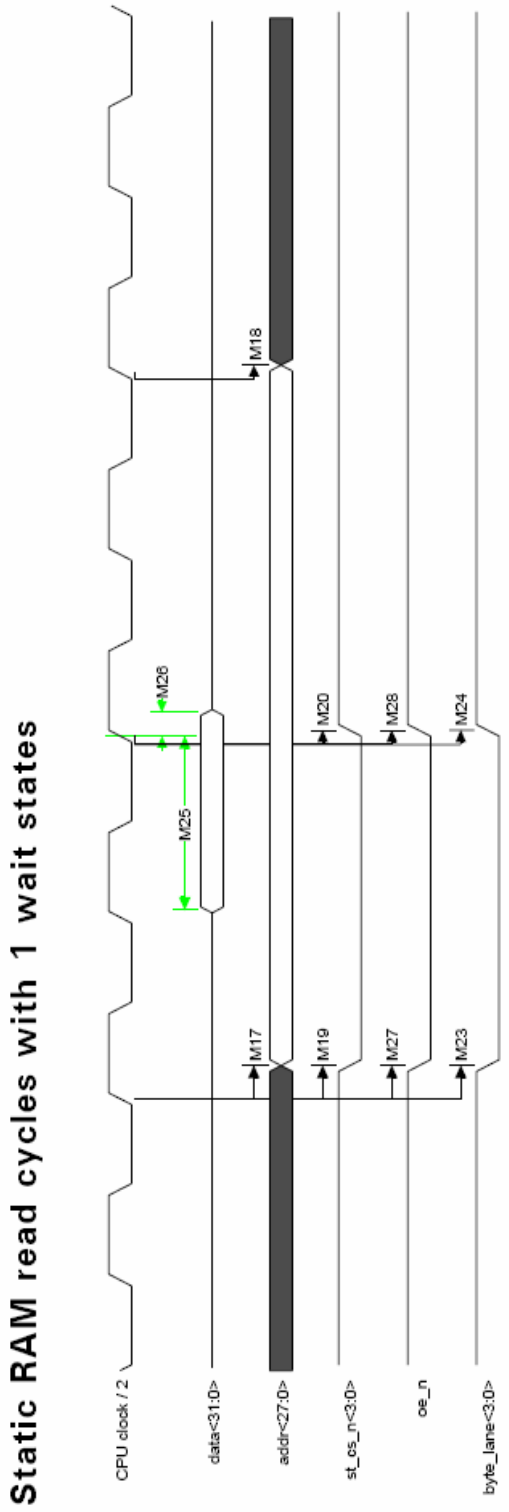


Figure 119: Static RAM read cycles with 1 wait state timing

- WTRD = 1
  WOEN = 0
- If the PB field is set to 1, all four `byte_lane` signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the `byte_lane` signal will always be high.

Figure 2 - Read Timing Diagram

10. Write Timing

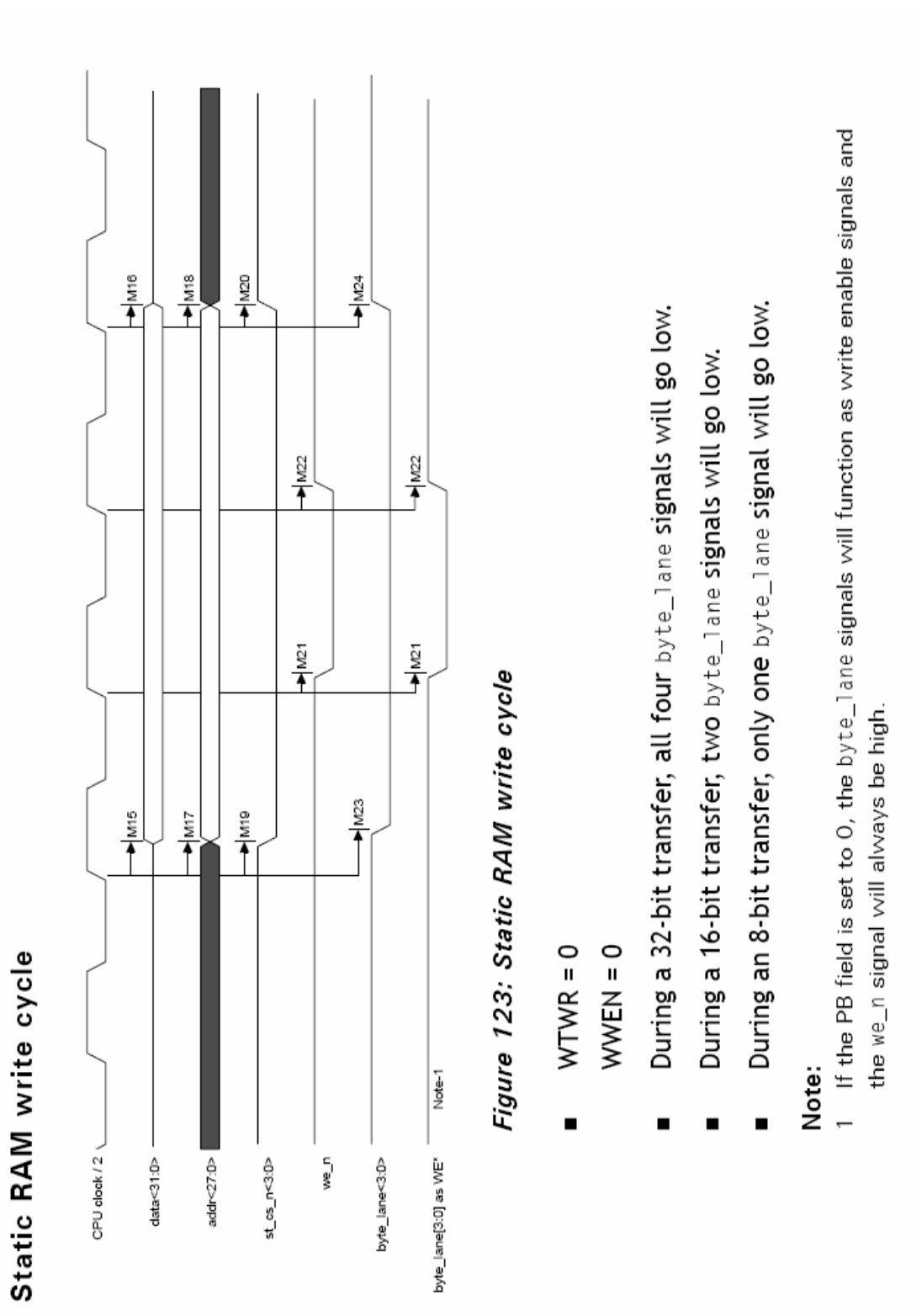


Figure 3 - Write Timing Diagram