Reset and Edge Sensitive Input

APPLICATION NOTE

Revisions:

Rev. A, 12/22/2005, Added Note 1 to exclude NS7520 *reset_n* from this rise time specification.

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Introduction

This application note provides information about the timing requirements for reset and edge sensitive inputs. The information is for board developers who use NetSilicon processors (*Note 1*).

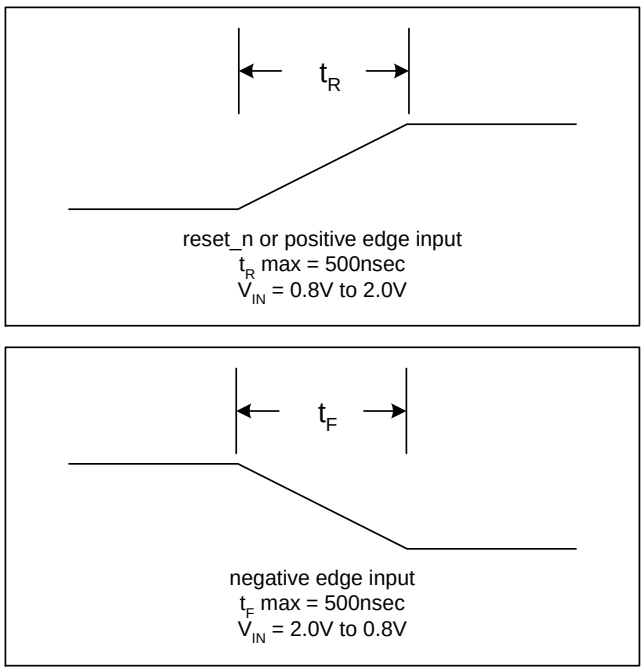
An example workaround is provided for applications for which the timing requirements cannot be met by a particular device output driving an edge sensitive input on a NetSilicon processors (*Note 1*).

Reset and edge sensitive input requirements

The critical timing requirement is the rise and fall time of the input:

- If the rise time is too slow for the reset input, the hardware strapping options may be registered incorrectly.
- If the rise time of a positive edge triggered external interrupt is too slow, an interrupt may be detected on both the rising and falling edge of the input signal.

To insure that reset and edge sensitive inputs are handled correctly, a maximum rise and fall time must be met. In the case of NetSilicon processors (*Note 1*), the maximum is 500 nanoseconds, as shown in these timing diagrams:



Workaround

If an external device driving the reset or edge sensitive input on a cannot meet the 500ns maximum rise and fall time requirement, the signal must be buffered with a Schmitt trigger device.

This table lists some example part numbers:

Manufacturer	Part number	Description
Fairchild	NC7SP17	Single Schmitt trigger buffer, available in 5-lead SC70 and 6-lead MicroPak package
Philips	74LVC1G17GW	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages
TI	SN74LVC1G17DCK	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages
ON Semi	NL17SZ17DFT2	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages

Note 1: NS7520 *reset_n* is excluded from this specification. See Netsilicon web site under; Support, Application Notes, – Recommended Errata Workarounds, File: "NS7520 Clock Speed Errata Application Note"