Document Type: Application Note

Document Name: Ethernet Receive Data FIFO Overflow Workaround for the NS9750 and NS9360

Change History:

Revision	Description	Date
1.0	Initial release	12/7/04
1.1	Added NS9360 to content. Updated logo and footers. Corrected bit name (REXEN → RXEN) in Step 3 of software workaround.	07/31/06

Description of Errata

The Ethernet receiver intermittently locks up in 100 Mbps half-duplex applications due to an overflow in the RX Data FIFO. The Ethernet Interrupt Status register indicates this condition by setting the RX_OVFL_DATA bit.

Software Workaround

Reset the RX Ethernet logic when an RX_OVFL_DATA interrupt is generated. The Ethernet driver should use these steps to recover from the stall condition.

1. Clear the ERX bit in Ethernet General Control Register #1.
2. Clear the ERXDMA bit in Ethernet General Control Register #1.
3. Clear the RXEN bit in MAC Configuration Register #1.
4. Clear the RX_OVFL_DATA bit in the Ethernet Interrupt Status register by writing a 1 to the bit.
5. If packets were received before the stall condition and are waiting to be serviced, service them as usual.
6. Reinitialize the Ethernet receive DMA rings.
7. Reload the RX Buffer Descriptor Pointer registers.
8. Clear the RXINIT bit in the Ethernet General Status register by writing a 1 to the bit.
9. Set the ERX bit in Ethernet General Control Register #1.
10. Set the ERXINIT bit in Ethernet General Control Register #1.
11. Wait for the RXINIT bit in the Ethernet General Status register to be set.
12. Clear the ERXINIT bit in Ethernet General Control Register #1.
13. Set the ERXDMA bit in Ethernet General Control Register #1.
14. Set the RXEN bit in MAC Configuration Register #1.

The Ethernet receive DMA indexes for all rings are reset to zero by the procedure. The Ethernet driver's internal variables must be updated accordingly before the driver services any packets after executing this procedure.